COMPAL CONFIDENTIAL

MODEL NAME : CAZ10

PCB NO : LA-E121P

BOM P/N : 431A4231L01

Steamboat 12" AR

Kabylake U

2016-04-25

REV : 0.1 (X00)

@ : Nopop Component

EMI@ : EMI Component
@EMI@ : EMI Nopop Component
ESD@ : ESDComponent
@ESD@ : ESD Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
CXDP@ : XDP Component
CONN@ : Connector Component
ESPI@ : ESPI interface Component
LPC@ : External ESPI Component (SHD)

MB PCB

Part Number	Description
DA800186000	PCB 1S5 LA-E121P REV0 MB AR 1

Layout Dell logo

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REV:X00
PWB:

Power CKT : 0425

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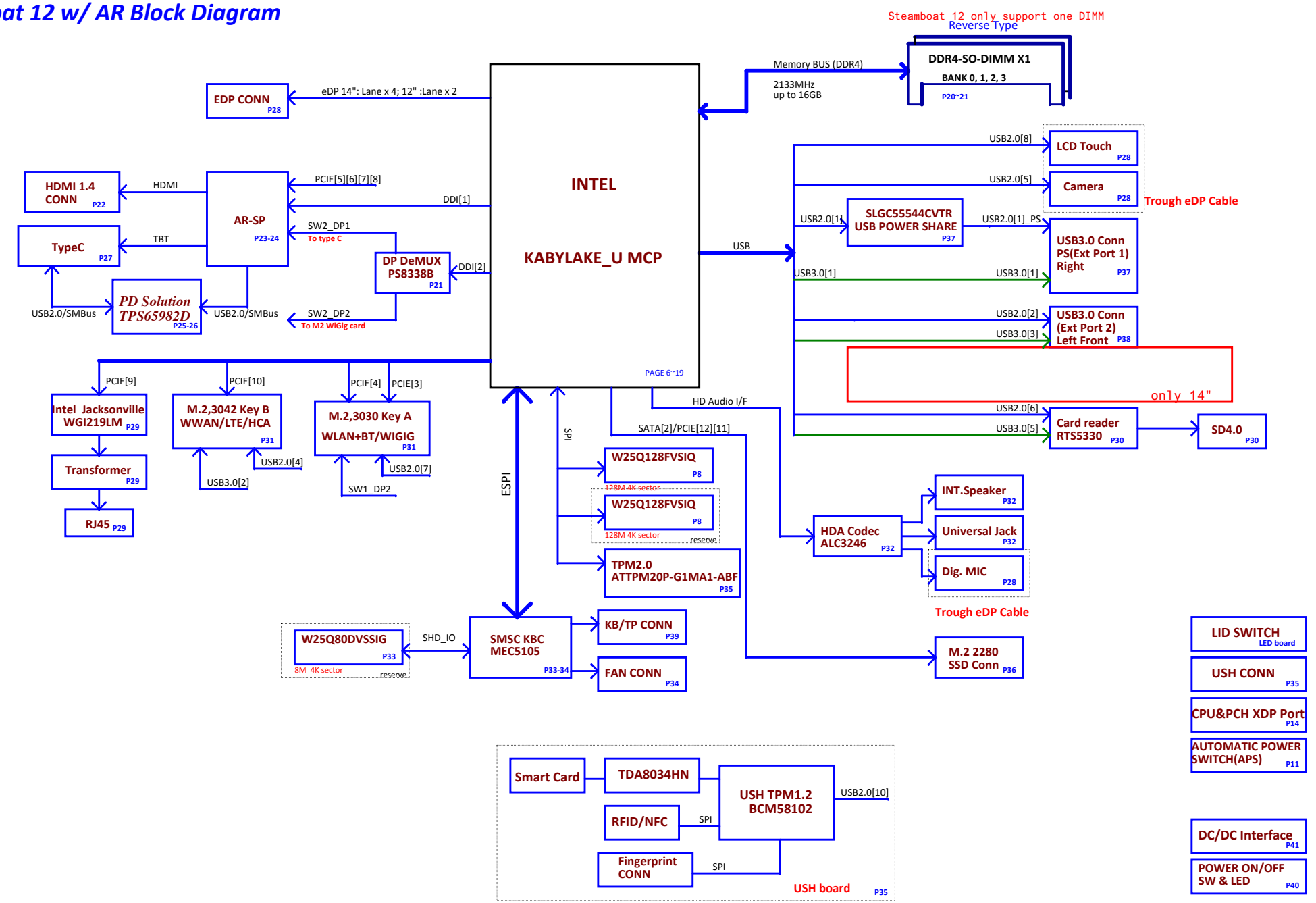
Title: Cover Sheet

Size: | Document Number: LA-E121P | Rev: 0.1

Date: Monday, April 25, 2016 | Sheet 1 of 52

Steamboat 12 w/ AR Block Diagram



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Title: Block diagram

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_DSW +3.3V_ALW_PCH +RTC_CELL +1.8V_PRIM +1.0V_PRIM +1.0V_PRIM_CORE +5V_ALW2 +3.3V_ALW2 +3.3V_RTC_LDO +1.0V_MPHYGT		
S0	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	GA-150LL	0.50
			Add Plating		0.95
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080 or1086	2.75
2	GND/PWR		Copper foil	0.5oz	0.60
		4	Core	4mil	4.00
3	Sig 1		Copper foil	0.5oz	0.60
		4.1	Prepreg	7628HRC	7.70
4	GND/PWR		Copper foil	1.0oz	1.25
		3.8	Core	4mil	4.00
5	Sig2		Copper foil	1.0oz	1.25
		4	Prepreg	7628	7.10
6	Sig3		Copper foil	0.5oz	0.60
		3.8	Core	4mil	4.00
7	GND/PWR		Copper foil	0.5oz	0.60
		3.7	Prepreg	1080 or1086	2.75
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		0.95
			SolderMask		0.50
Overall Thickness (1.0mm +-10%)			39.4		41.40000
					1.05156

AR use 1086PP
Non AR use 1080PP

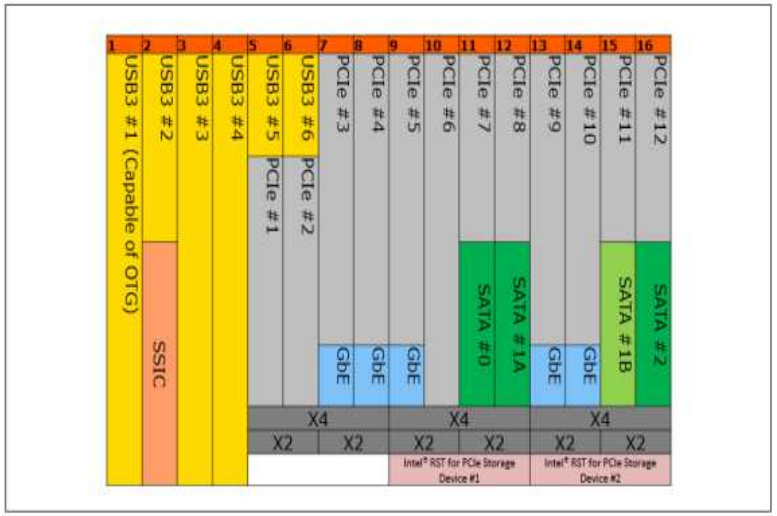
USB3.0	SSIC	PCIE	SATA	DESTINATION
USB3.0-1				JUSB1-->Right
USB3.0-2	SSIC			M.2 3042(LTE)
USB3.0-3				JUSB2-->Left Front
USB3.0-4				JUSB3-->Left Rear (SB14 only)
USB3.0-5		PCIE-1		Card Reader
USB3.0-6		PCIE-2		NA
		PCIE-3		M.2 3030(WLAN)
		PCIE-4		M.2 3030(WIGIG)
		PCIE-5		Alpine Ridge - SP
		PCIE-6		
		PCIE-7	SATA-0	
		PCIE-8	SATA-1	
		PCIE-9		LOM
		PCIE-10		M.2 3042(HCA)
		PCIE-11	SATA-1*	M.2 2280 SSD (PCIex2 or SATA)
		PCIE-12	SATA-2	

12" not support JUSB3

USB PORT#	DESTINATION
1	JUSB1-->Right
2	JUSB2-->Left Front
3	JUSB3-->Left Rear (SB14 only)
4	M2 3042(WWAN)
5	Camera
6	Card Reader
7	M.2 3030(BT)
8	Touch Screen
9	NA
10	USH

AR config

High Speed I/O (HSIO) Lane Multiplexing in KBL U



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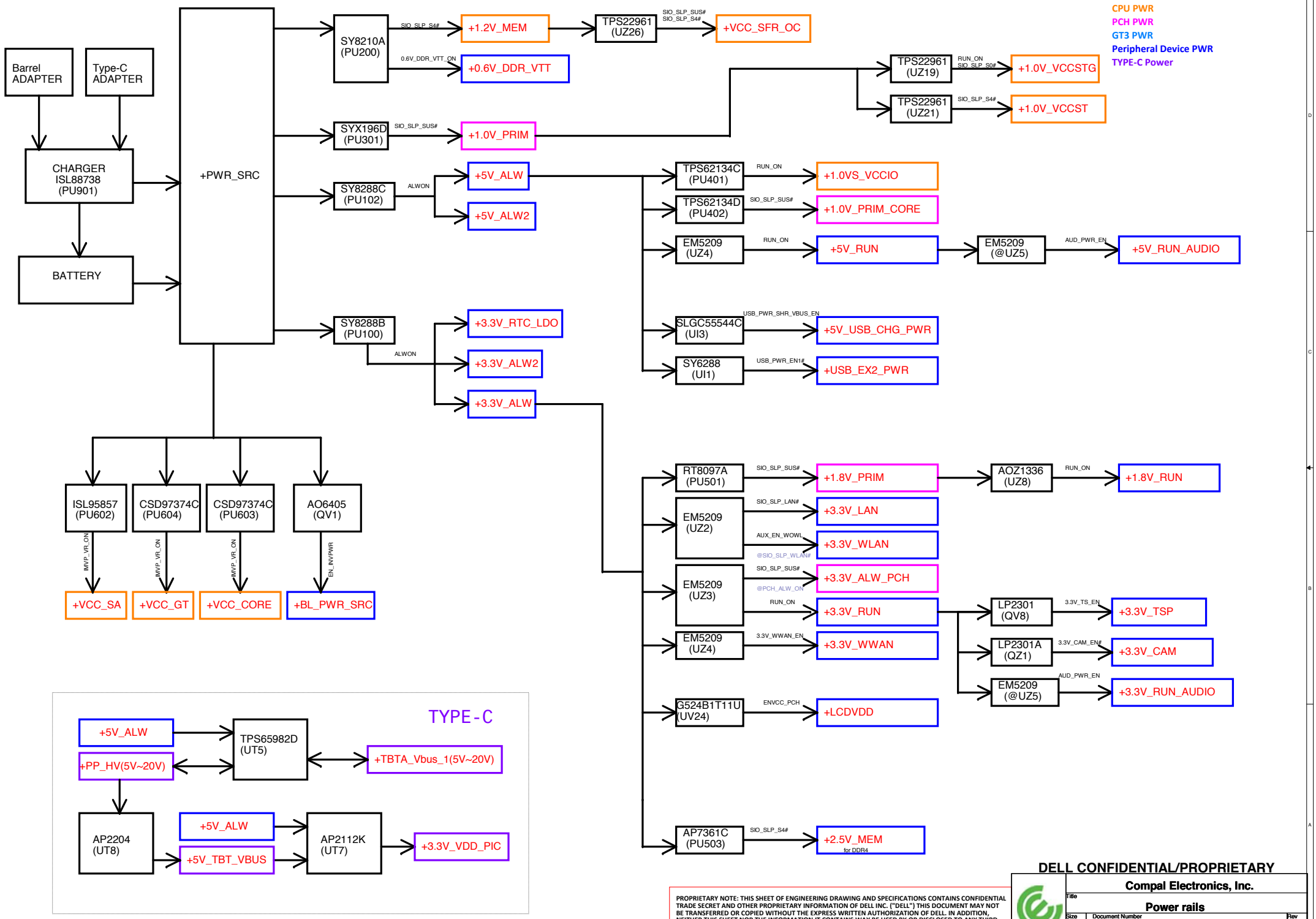
Title: Port assignment

Size | Document Number: LA-E121P | Rev: 0.1

Date: Monday, April 25, 2016 | Sheet 3 of 52



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Compal Electronics, Inc.

Title: Power rails

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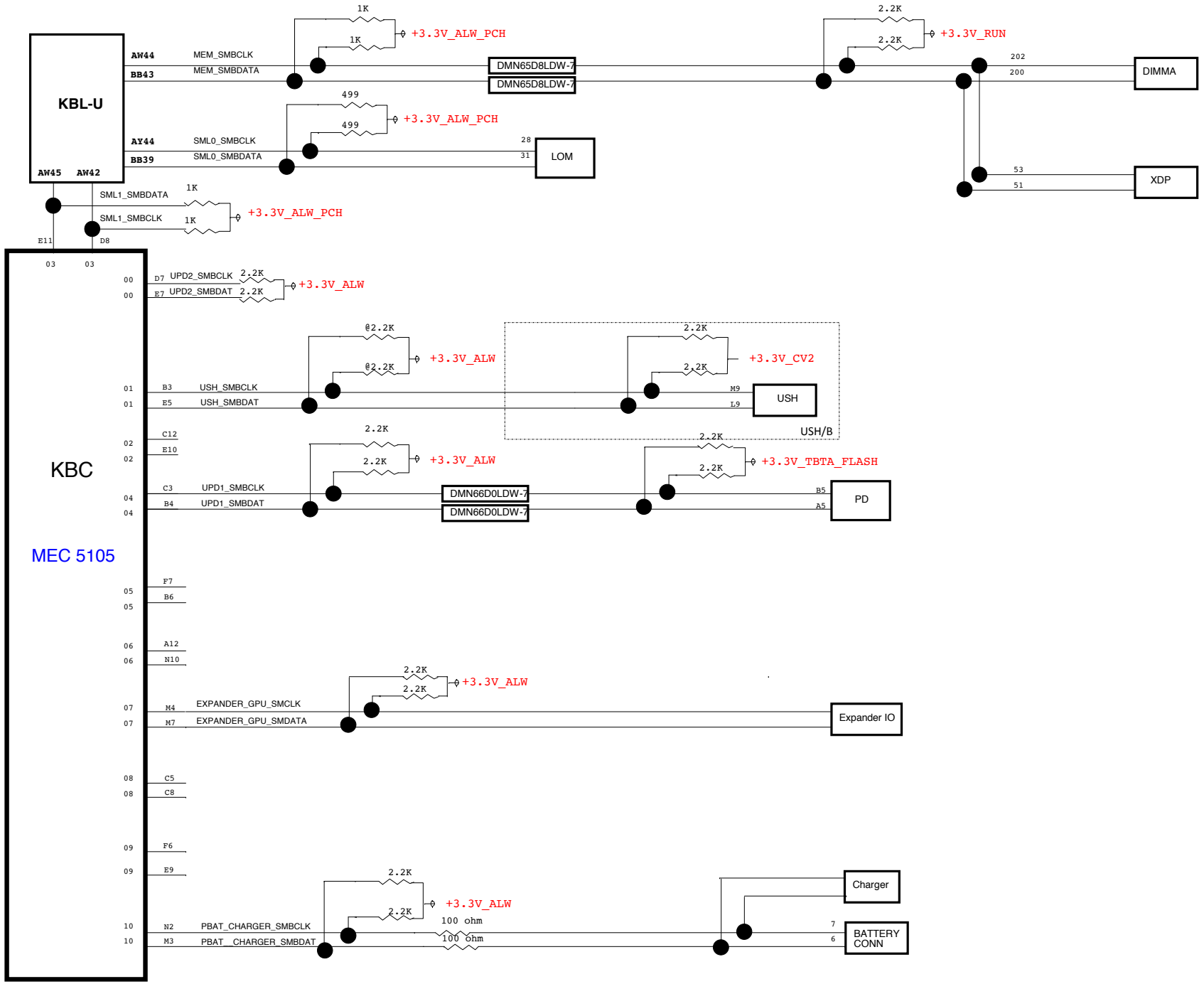

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Title: Port assignment

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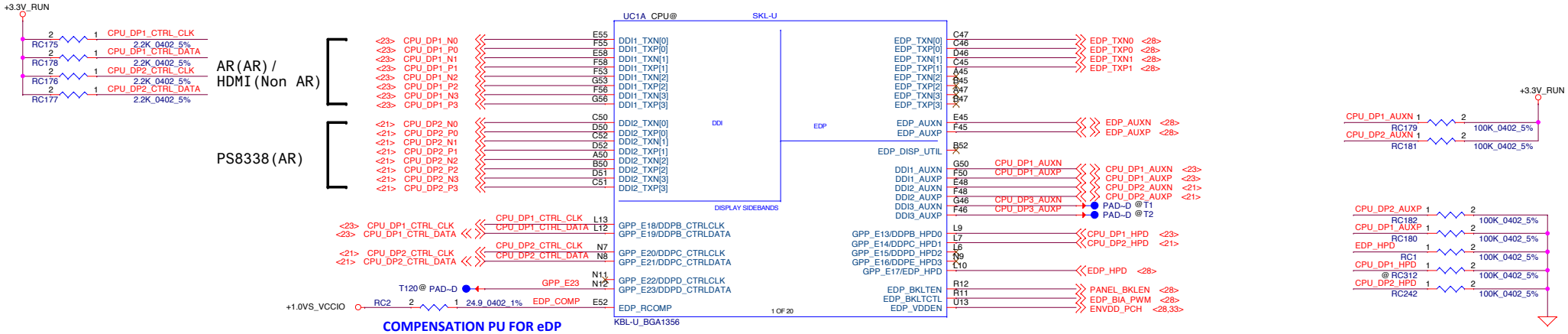
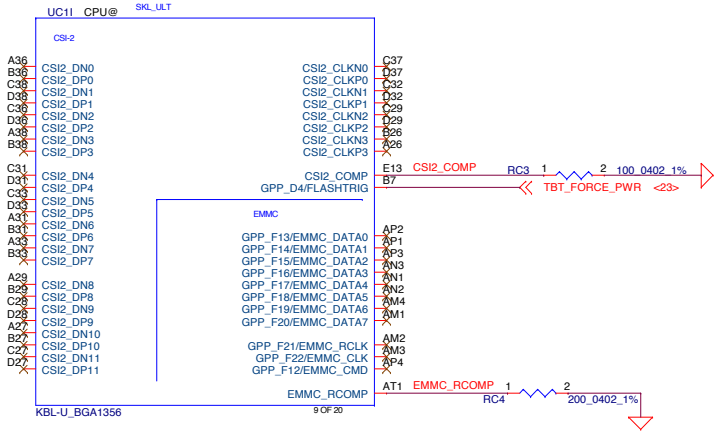


COMPENSATION PU FOR eDP

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

SKL-U Ballout Rev0.71 & INTEL symbol Rev1.0



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Title: CPU (1/14)

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For DDR4

DDR4, Ballout for side by side(Interleave)

DDR4 COMPENSATION SIGNALS

SM_RCOMP0 RC5 1 2 121_0402_1%
SM_RCOMP1 RC6 1 2 80.6_0402_1%
SM_RCOMP2 RC7 1 2 100_0402_1%

CAD Note:
Trace width=12~15 mil, Spacing=20 mils
Max trace length= 500 mil

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Title: CPU (2/14)
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SPI_MOSI= SPI_IO0
SPI_MISO= SPI_IO1
PCH EDS R0.7 p.235~236

For BR/SB

UC1E CPU@ SKL-U

KBL-U_BGA1356

5 OF 20

+1.8V?

CHECK LPC_CLK FOR DEBUG CARD?

SOFTWARE TAA

03/02:follow Intel MOW_2015WW06

RF Request

Place close CPU side

128Mb Flash ROM

W25Q128FVSIQ_SO8

E-T_6705K-Y20N-00L

JSPI1 CONN@

TLS CONFIDENTIALITY

HIGH	ENABLE
LOW(DEFAULT)	DISABLE

WEAK INTERNAL 20K PD

EC interface

HIGH	ESPI
LOW(DEFAULT)	LPC

WEAK INTERNAL 20k PD

EXI BOOT STALL BYPASS

HIGH	ENABLED
LOW(DEFAULT)	DIABLED

WEAK INTERNAL PD

Reserve

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Title: CPU (3/14)

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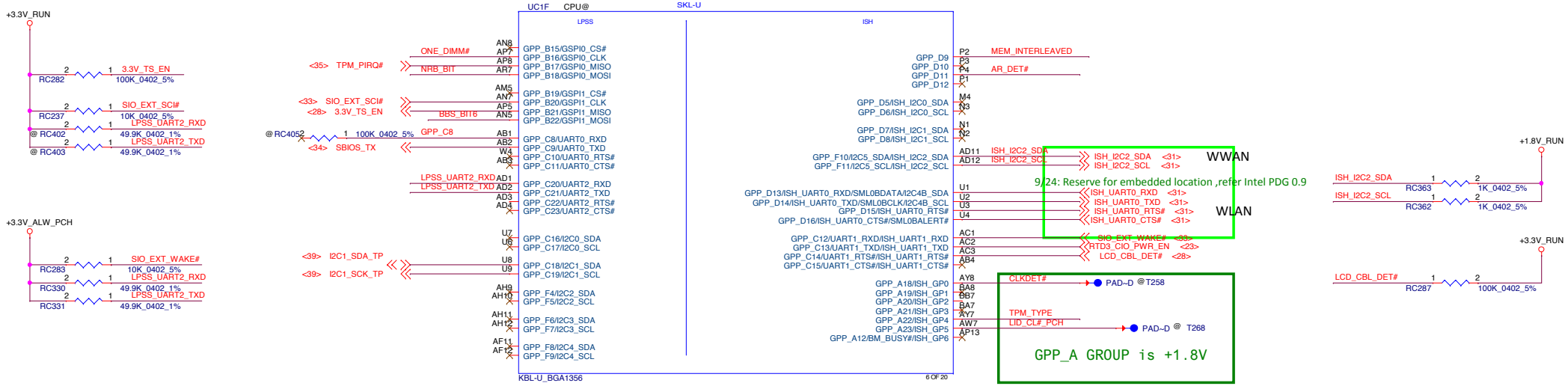
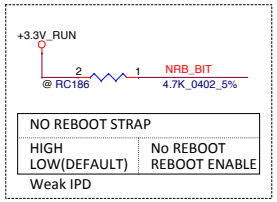
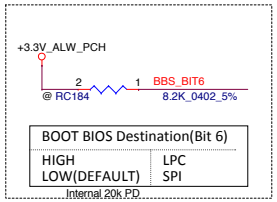
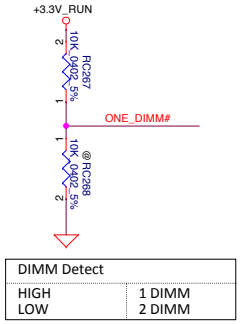
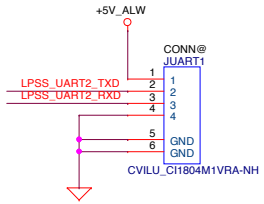
For BR/SB

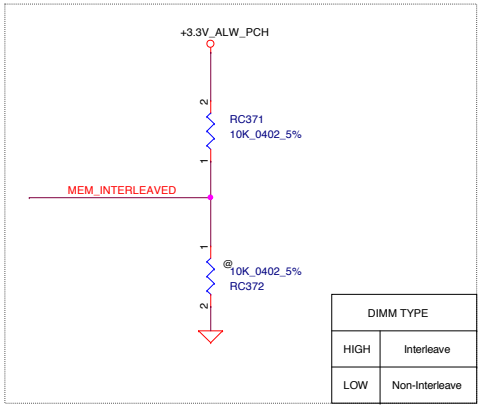


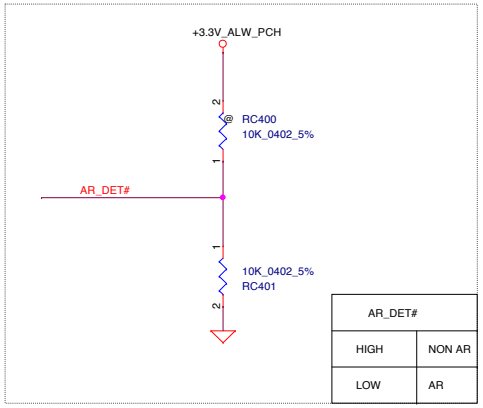












Reserved TPM_TYPE @ RC349 100_0402_1%

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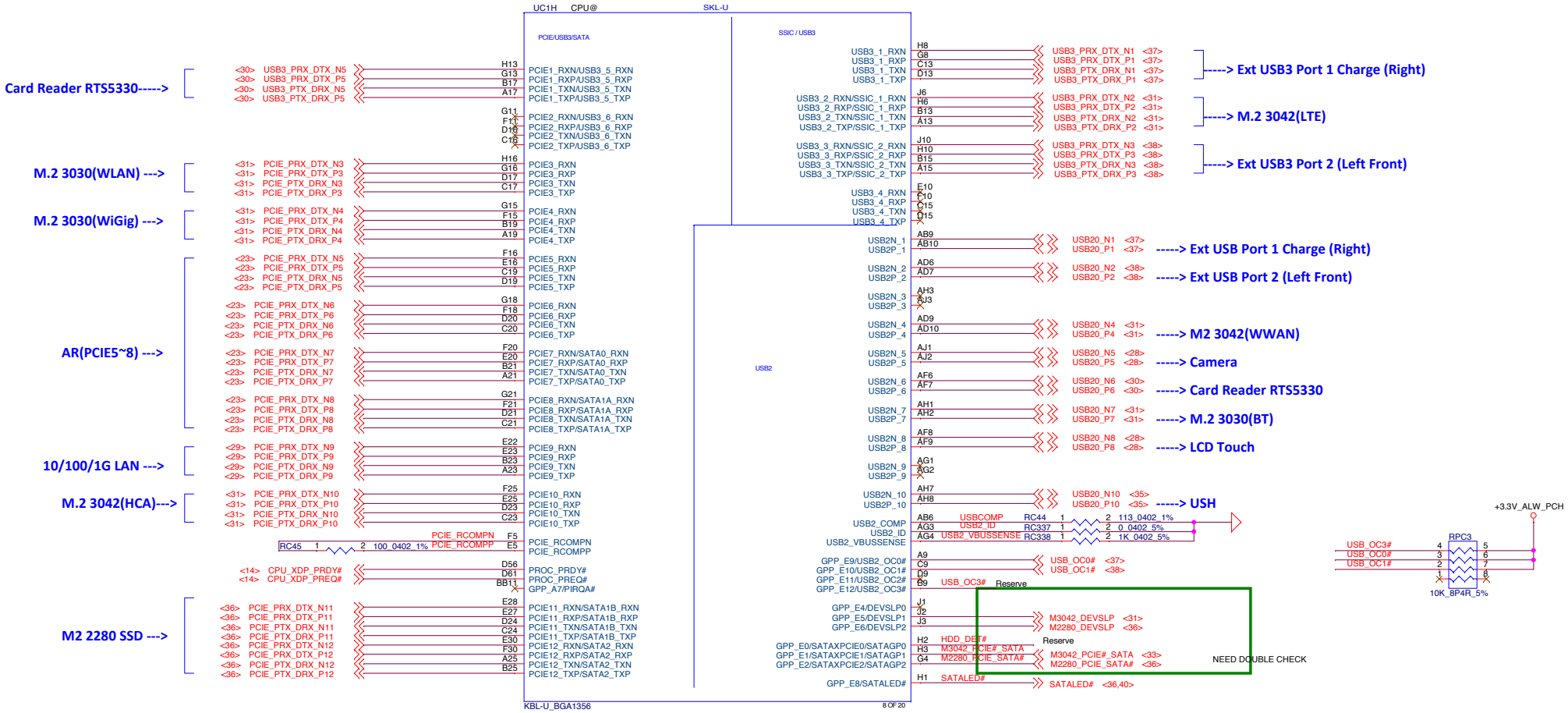
For AR,Steamboat12/14



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Compal Electronics, Inc.		
Title: CPU (5/14)		
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For SB/KW UMA w AR

WWAN--->
WLAN--->
WIGIG--->
M.2 SDD--->
LAN--->
AR --->

UC1J CPU@ SKL_ULT

CLOCK SIGNALS

KBL-U_BGA1356

10 OF 20

CMOS1 must take care short & touch risk on layout placement

SHORT PADS~D @CMOS1

YC1 24MHZ_12PF_X3G024000DC1H

For Skylake,YC1 24 MHz (50 Ohm ESR)
For Cannonlake,YC1 38.4 MHz (30 Ohm ESR)
546765_546765_2014WW48_Skylake_MOW_Rev_1_0

YC2 32.768KHZ_12.5PF_9H03200042
ESR MAX=50k ohm

For Skylake, pop RC52,depop RC324
For Cannonlake, pop RC324,depop RC52

8/21 can change to 10K for merge to RP

UC7 TC7SH08FU_SSOP5~D

UC1K CPU@ SKL-U

SYSTEM POWER MANAGEMENT

KBL-U_BGA1356

11 OF 20

connect to VCCMPHYGTAON_1P0 enable pin

ESD Request:place near CPU side

RC215	
POP	NO Support Deep sleep
DE-POP	Support Deep sleep

if pop UC12, RC291 also need pop(74AHC1G09GW is OD output)

JAPS1 CONN@ CVILU_CF4218FH0R0-05-NH

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Compal Electronics, Inc.

Title: CPU (6/14)

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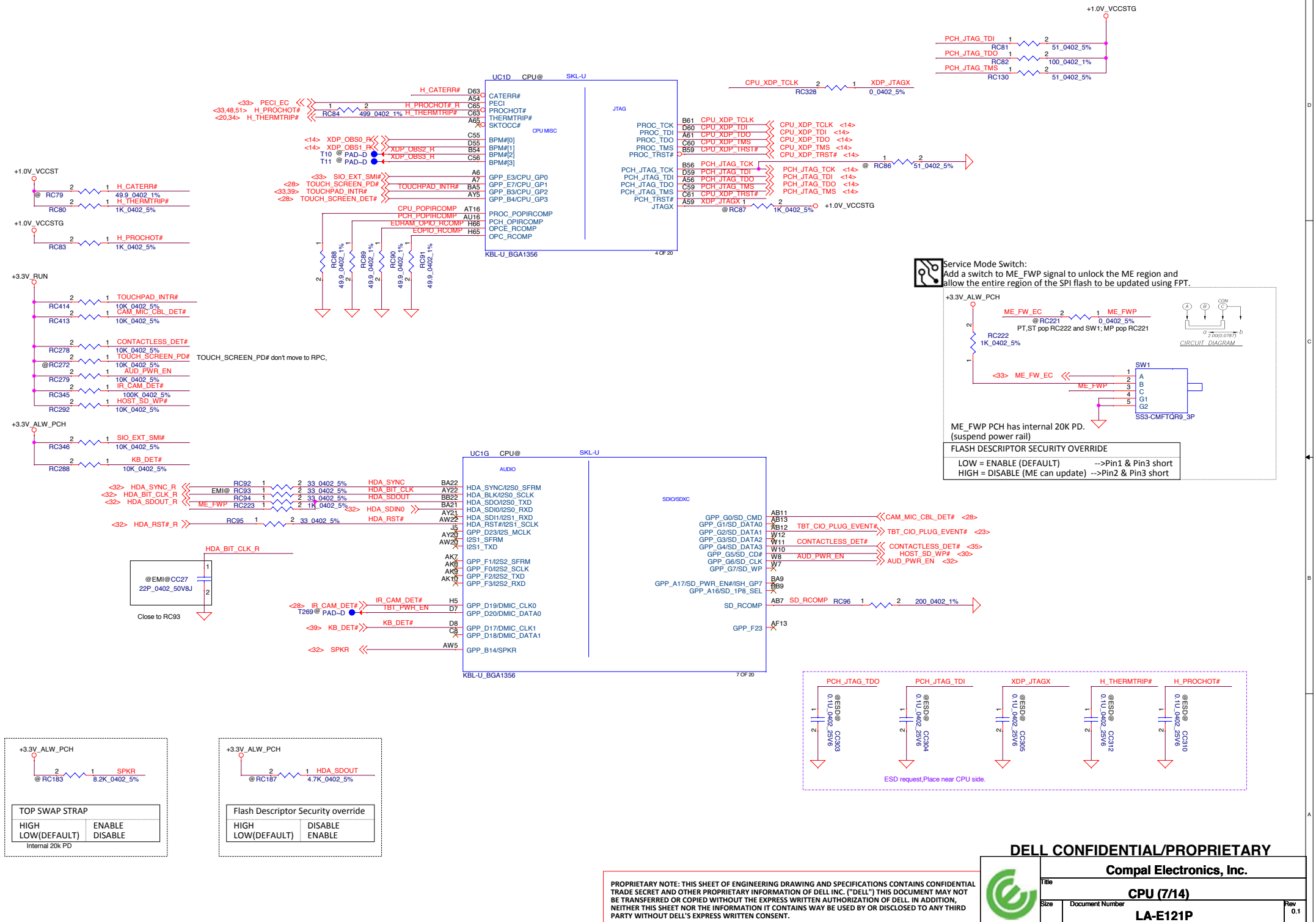

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Compal Electronics, Inc.

Title: CPU (7/14)

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<14> CFG[0..19]

CFG[2][5][6][7] for SKYLAKE-H CPU CFG strap pin

2 1 CFG0
@ RC113 10K_0402_1%

Stall reset sequence	
HIGH(DEFAULT)	No stall(Normal Operation)
LOW	stall

2 1 CFG4
RC109 1K_0402_5%

eDP enable	
HIGH(DEFAULT)	Disabled
LOW	Enabled

2 1 10K_0402_1% @ RC112
2 1 10K_0402_1% @ RC110

UC1S_CPU@ SKL-U
RESERVED SIGNALS-1

CFG0 E68 CFG[0]
CFG1 B67 CFG[1]
CFG2 D65 CFG[2]
CFG3 D67 CFG[3]
CFG4 E70 CFG[4]
CFG5 C68 CFG[5]
CFG6 D68 CFG[6]
CFG7 C67 CFG[7]
CFG8 F71 CFG[8]
CFG9 G69 CFG[9]
CFG10 F70 CFG[10]
CFG11 G68 CFG[11]
CFG12 H70 CFG[12]
CFG13 G71 CFG[13]
CFG14 H69 CFG[14]
CFG15 G70 CFG[15]
CFG16 E63 CFG[16]
CFG17 F63 CFG[17]
CFG18 E66 CFG[18]
CFG19 F66 CFG[19]

2 1 CFG_RCOMP E60 CFG_RCOMP
RC114 49.9_0402_1%
+1.0V_PRIM_XDP 2 1 ITP_PMODE E8 ITP_PMODE
RC115 1.5K_0402_5%
<14> ITP_PMODE

AY2 RSVD_AY2
AY1 RSVD_AY1
D1 RSVD_D1
D3 RSVD_D3
K46 RSVD_K46
K45 RSVD_K45
AL25 RSVD_AL25
AL27 RSVD_AL27
C71 RSVD_C71
B70 RSVD_B70
F60 RSVD_F60
A52 RSVD_A52
BA70 RSVD_TP_BA70
BA68 RSVD_TP_BA68
J71 RSVD_J71
J68 RSVD_J68
F65 VSS_F65
G65 VSS_G65
F61 RSVD_F61
E61 RSVD_E61

T16 @ PAD~D
T17 @ PAD~D

BB68 RSVD_TP_BB68 PAD~D @T12
BB69 RSVD_TP_BB69 PAD~D @T13
AK13 RSVD_TP_AK13 PAD~D @T14
AK12 RSVD_TP_AK12 PAD~D @T15
BB2 RSVD_BB2
BA3 RSVD_BA3
AU5 TP5 PAD~D @T128
AT5 TP6 PAD~D @T129
D5 RSVD_D5
D4 RSVD_D4
B2 RSVD_B2
C2 RSVD_C2
B3 RSVD_B3
A3 RSVD_A3
AW1 RSVD_AW1
E1 RSVD_E1
E2 RSVD_E2
BA4 RSVD_BA4
BB4 RSVD_BB4
A4 RSVD_A4
C4 RSVD_C4
BB5 TP4 PAD~D @T130
A69 RSVD_A69
B69 RSVD_B69
AY3 RSVD_AY3
D71 RSVD_D71
C70 RSVD_C70
C54 RSVD_C54
D54 RSVD_D54
AY4 TP1 PAD~D @T126
BB3 TP2 PAD~D @T127
AY71 VSS_AY71
AR56 ZVM#
AW71 RSVD_TP_AW71 PAD~D @T113
AW70 RSVD_TP_AW70 PAD~D @T114
AP56 MSM#
C64 PROC_SELECT#
1 2 100K_0402_5% @ RC120 +1.0V_VCCST

For Skylake , RC120 depop
For Cannonlake, RC120 pop

19 OF 20
KBL-U_BGA1356

1/5 2014WW52 MOW reserve to support Cannonlake-U PCH compatibility
close UC1.U11/U12 and <400mil

+1.8V_PRIM 1 2 0_0402_5% @ RC313 +VCC_1P8
1 2 1U_0402_6.3V6K @ CC222

UC1T SKL-U
SPARE

AW69 RSVD_AW69 F6 RSVD_F6
AW68 RSVD_AW68 E3 RSVD_E3
AU56 RSVD_AU56 C11 RSVD_C11
AW48 RSVD_AW48 B11 RSVD_B11
C7 RSVD_C7 A11 RSVD_A11
U12 RSVD_U12 D12 RSVD_D12
U11 RSVD_U11 C12 RSVD_C12
H11 RSVD_H11 F52 RSVD_F52

20 OF 20
KBL-U_BGA1356

ZVM# for SKYLAKE-U 2+3e

MSM# for SKYLAKE-U 2+3e

546765_546765_2014WW48_Skylake_MOW_Rev_1_0

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Compal Electronics, Inc.
Title: CPU (8/14)
Size: Document Number: LA-E121P
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Date: Monday, April 25, 2016
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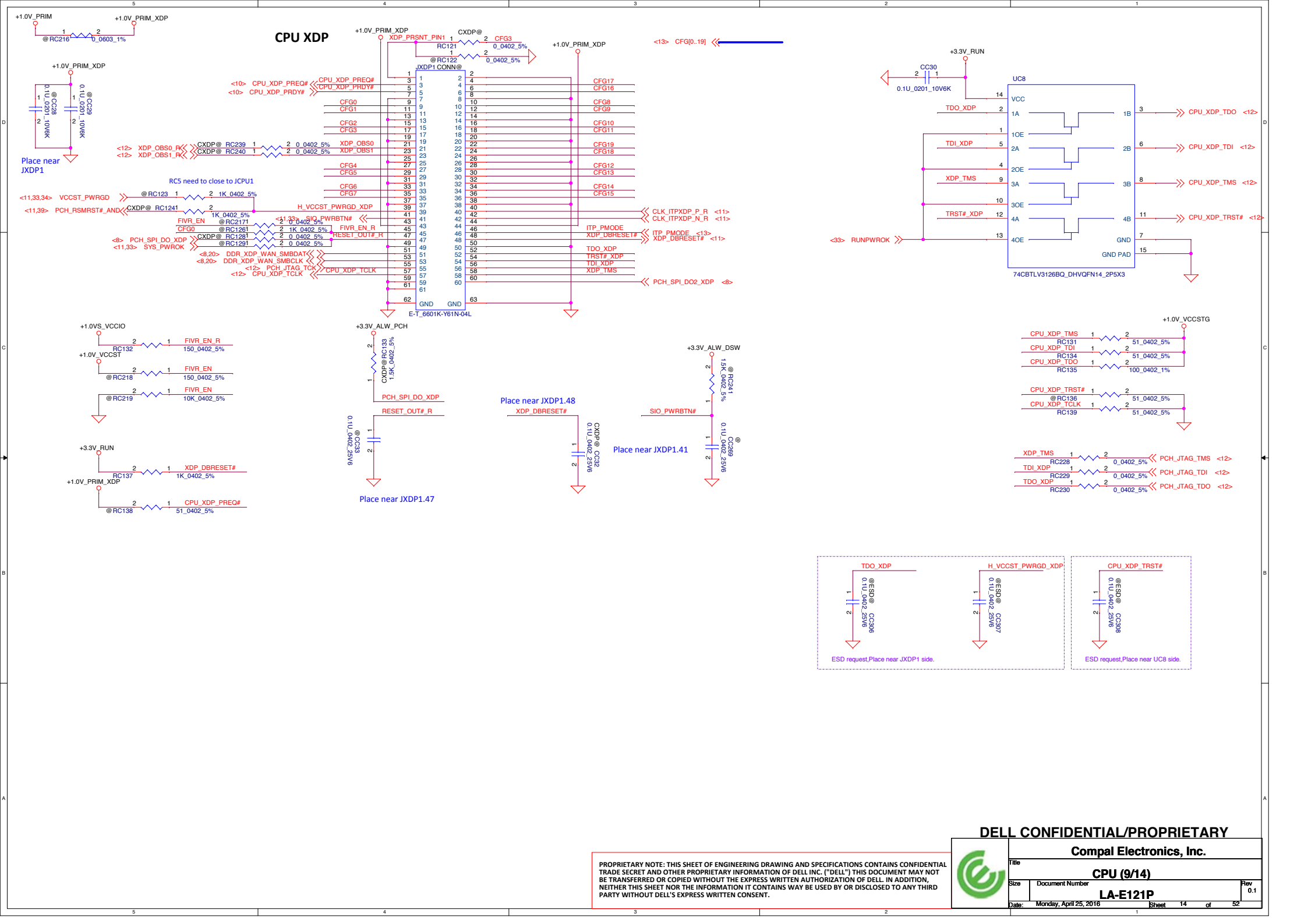

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Compal Electronics, Inc.

Title: CPU (9/14)

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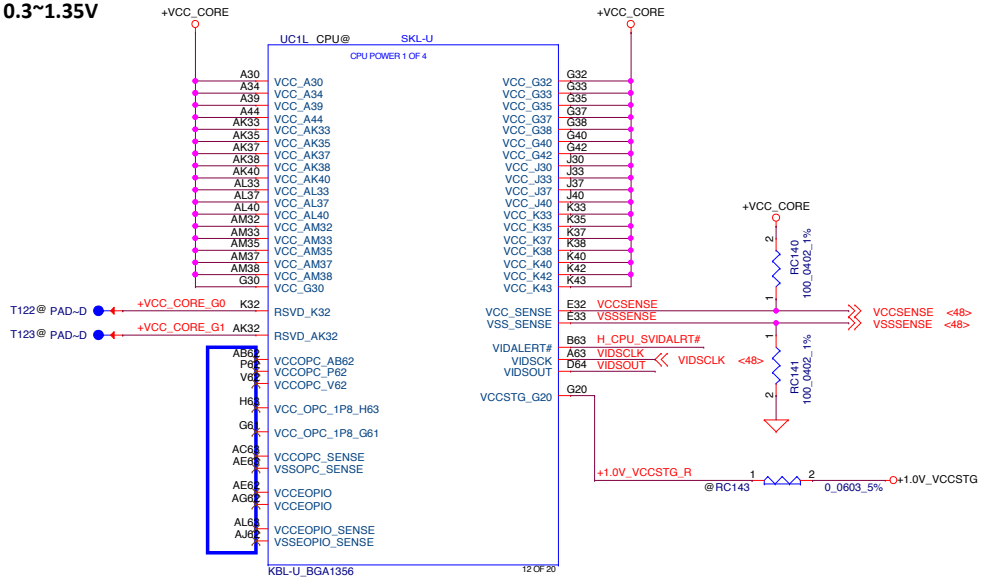
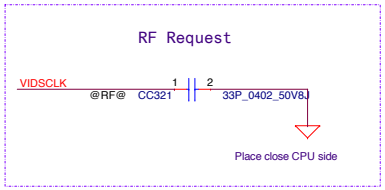
+VCC_CORE: 0.3~1.35V

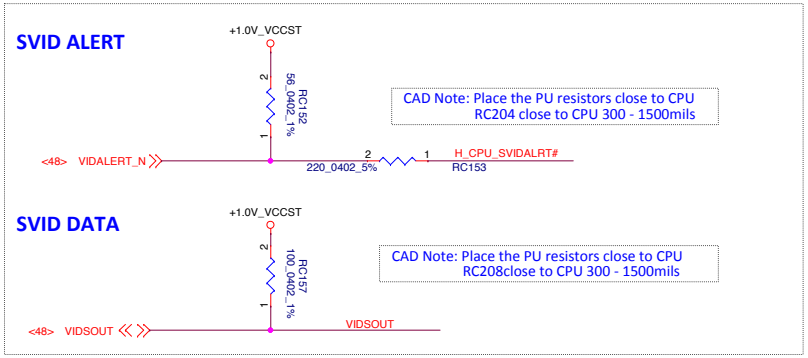


PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps >Power source

VCCOPC,VCCOPC_1P8,VCCEOPIO for SKYLAKE-U 2+3e (w/ on package cache)





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Compal Electronics, Inc.

Title: CPU (10/14)

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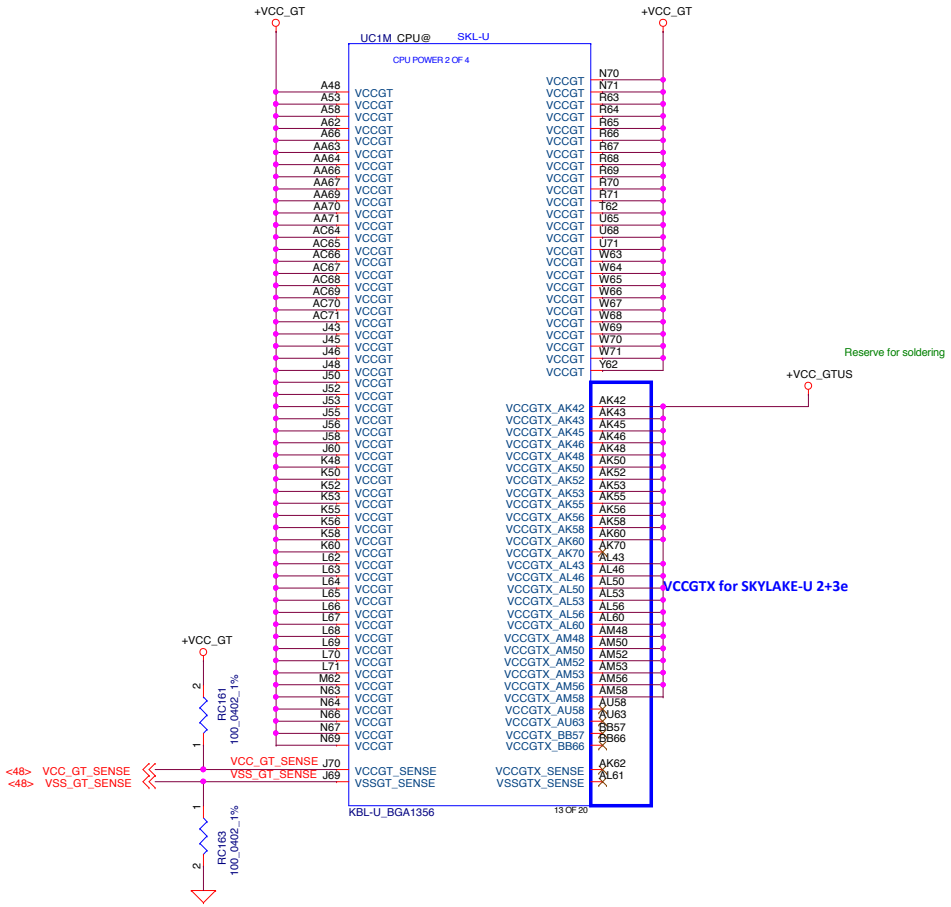
+VCCGT: 0.3~1.35V
+VCCGTX : 0.3~1.35V



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Compal Electronics, Inc.		
Title: CPU (11/14)		
Size	Document Number: LA-E121P	Rev: 0.1
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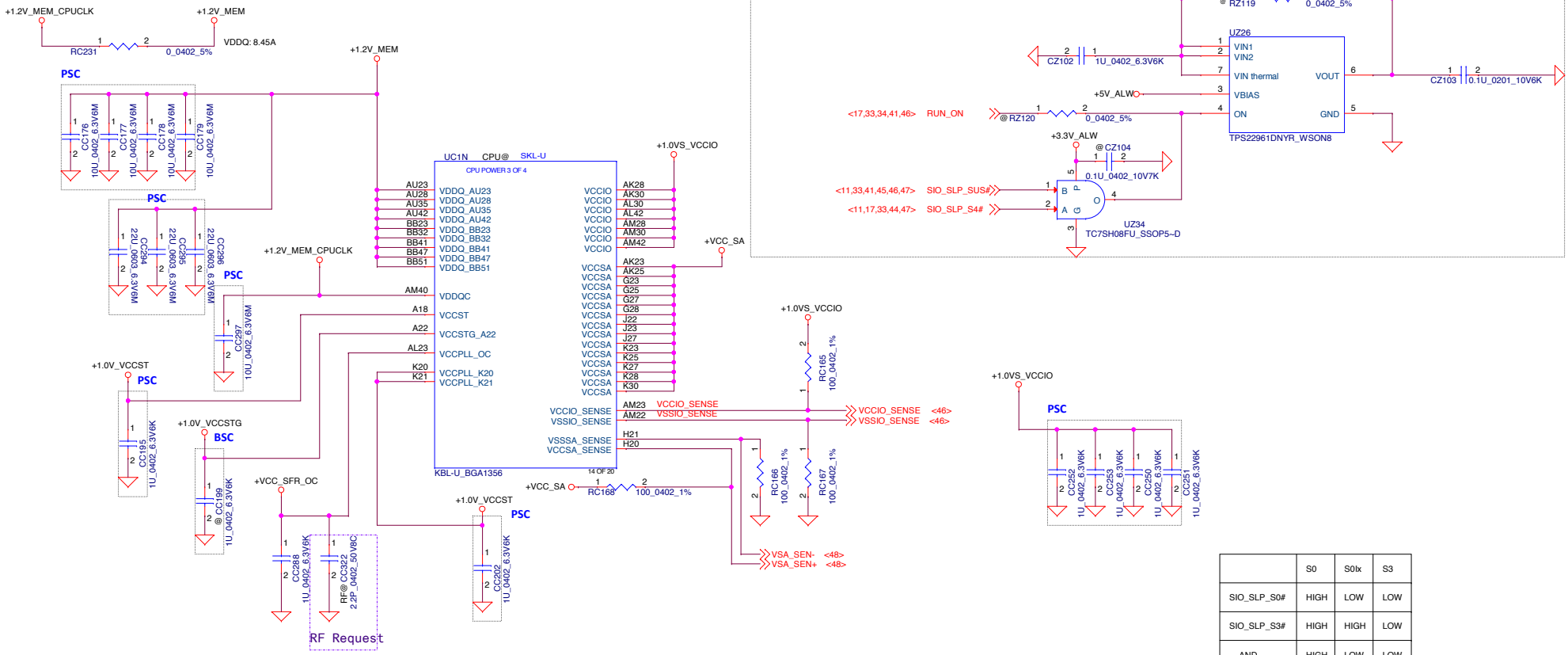
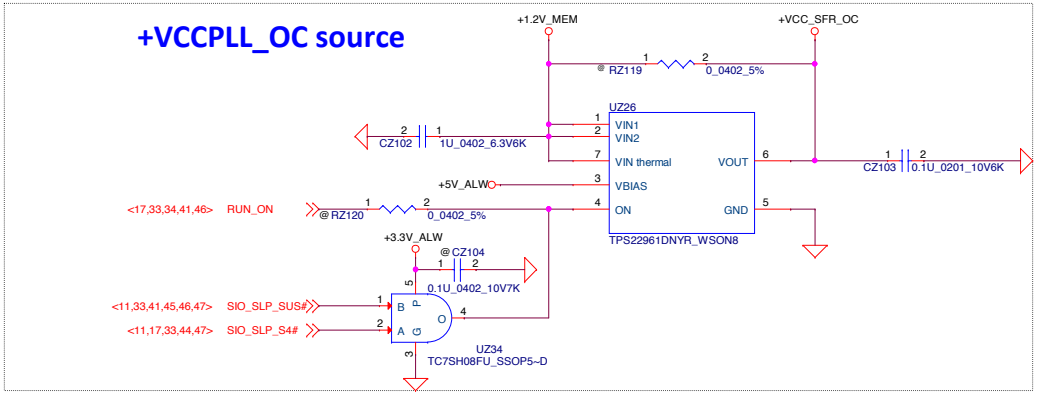
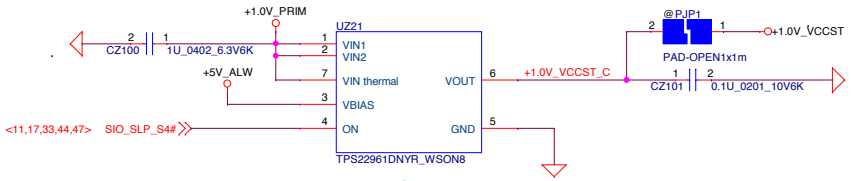


+VCCPLL_OC source

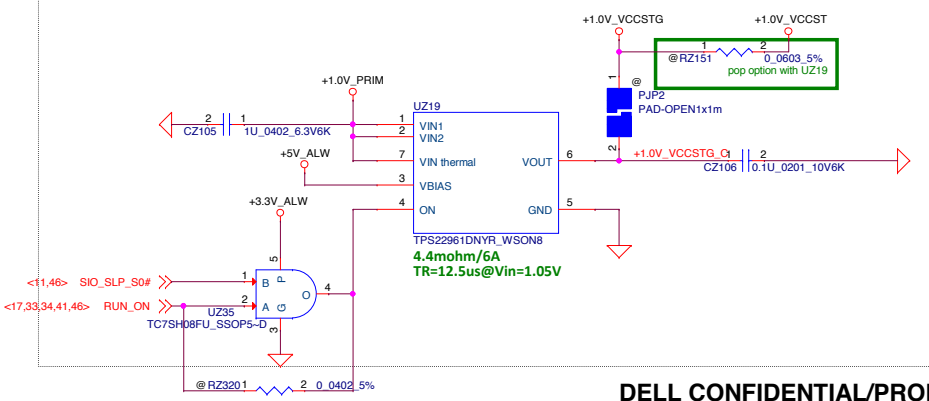


	S0	S0Ix	S3
SIO_SLP_S0#	HIGH	LOW	LOW
SIO_SLP_S3#	HIGH	HIGH	LOW
AND	HIGH	LOW	LOW

+1.0V_VCCST source



+1.0V_VCCSTG source



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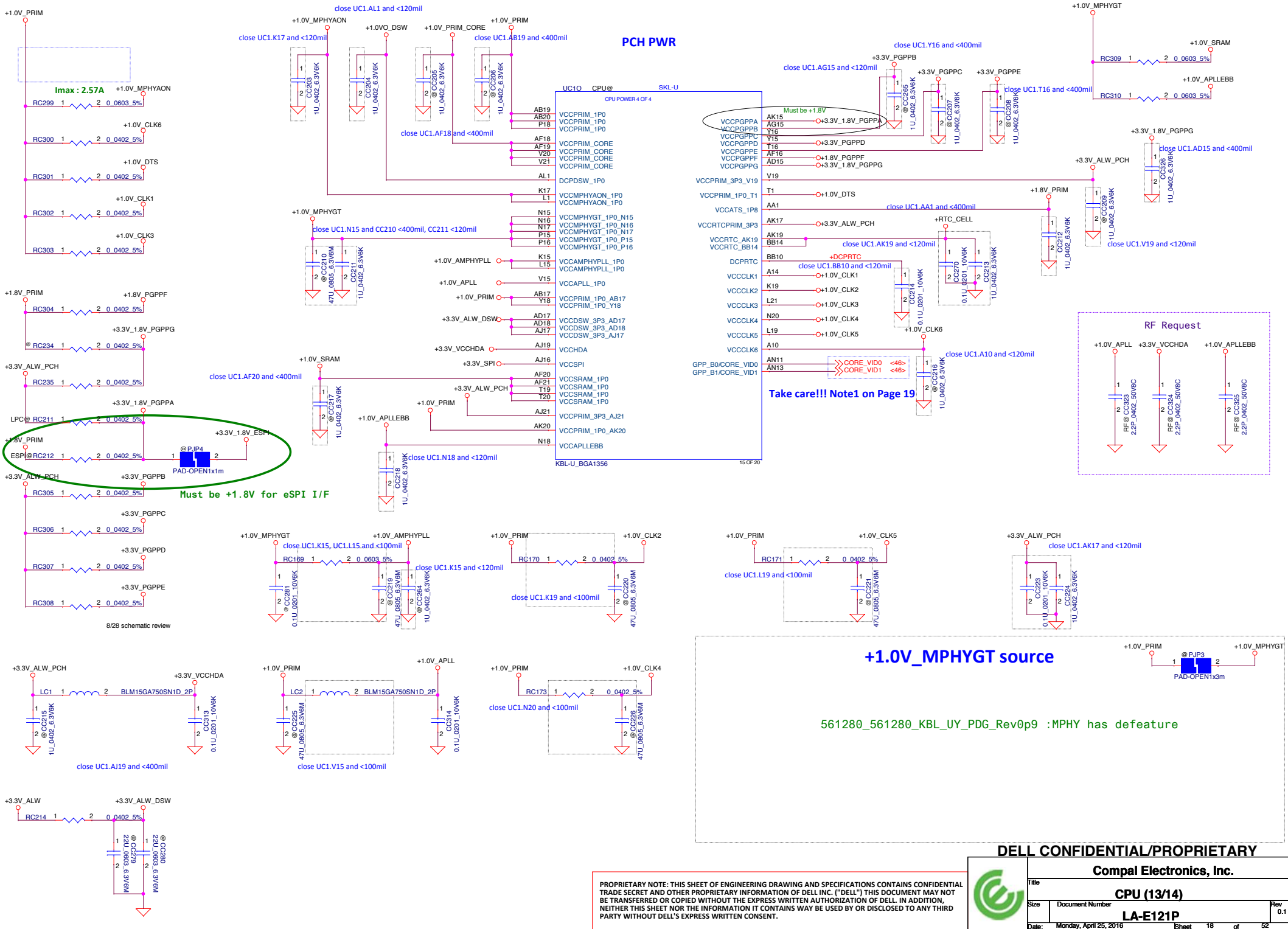
Compal Electronics, Inc.

Title: CPU (12/14)

Size | Document Number: LA-E121P | Rev: 0.1

Date: Monday, April 25, 2016 | Sheet 17 of 52



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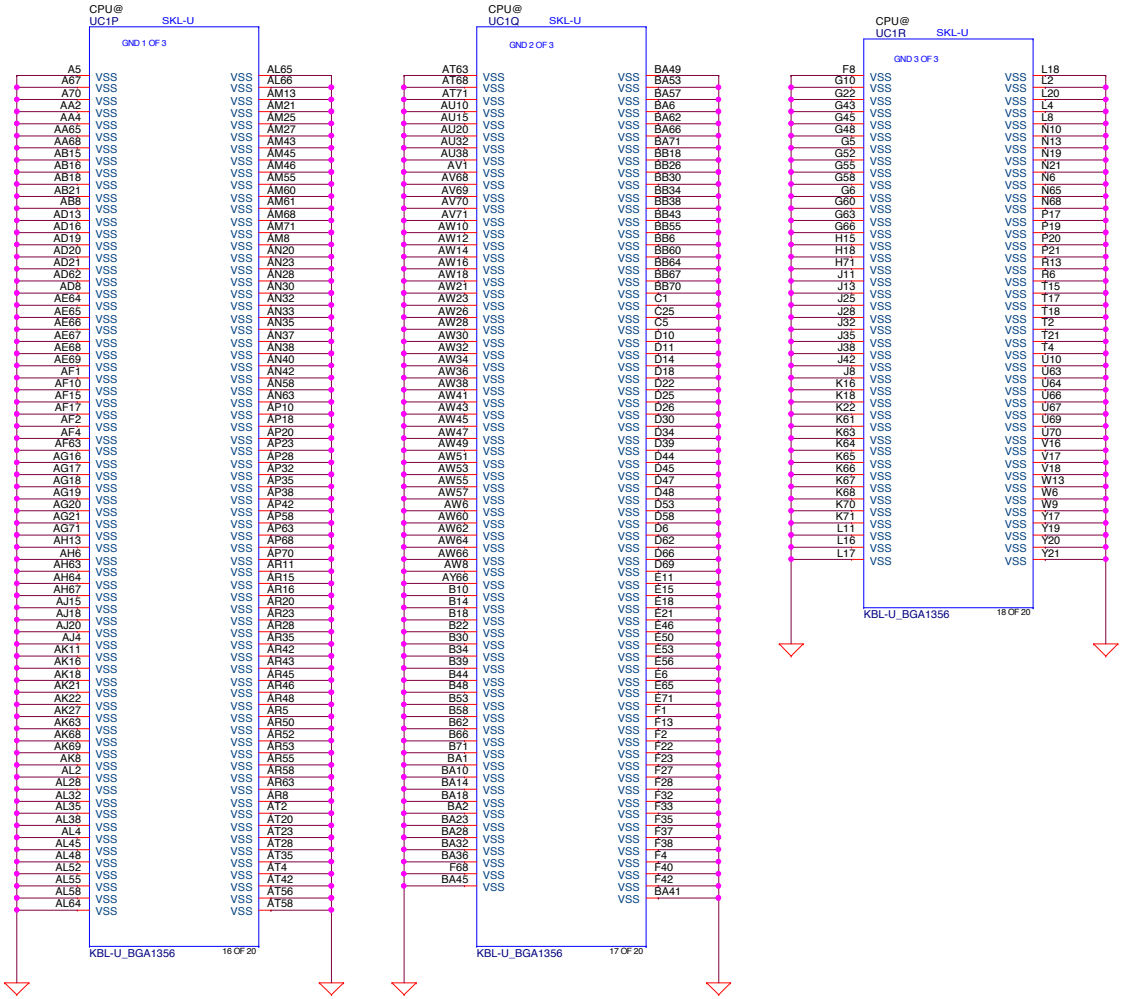
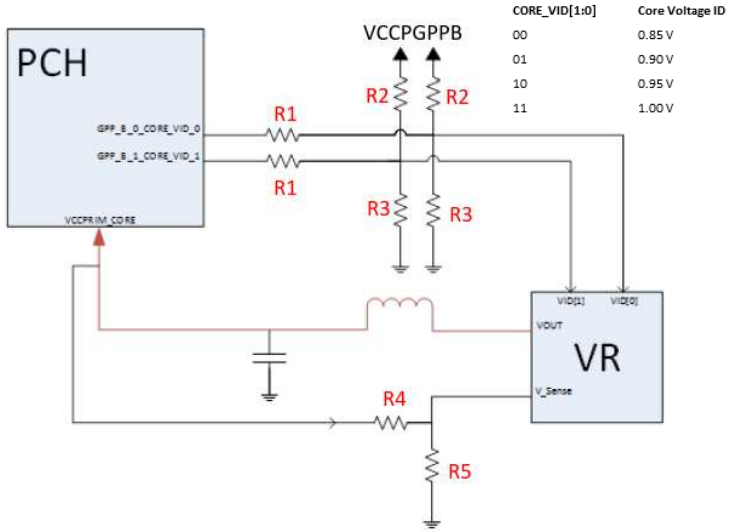


Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

R1: PR408,PR411 ; R2: PR417,PR418 ; R3,PR419,PR420 ; R4: PR423 ; R5: PR424



CORE_VID[1:0]	Core Voltage ID
00	0.85 V
01	0.90 V
10	0.95 V
11	1.00 V

For Pre-ES Parts: Disconnect PCH CORE_VID[1:0] to the VR and fix PCH VCCPRIM_CORE voltage at 1.00 V.

- R1: not populated
- R2, R3: populated to set VCCPRIM_CORE to 1.00V. Consult with VR vendor for appropriate values.
- R4, R5 (feedback resistor): populated if needed. Some VRs only support up to 0.95V natively with VID options. 1.00 V should be created by selecting 0.95V option and using feedback resistors to shift voltage up 50 mV. Consult with VR vendor for appropriate values for proper VR operation while minimizing power consumption

For ES and Later Parts: Connect PCH CORE_VID[1:0] to the VR.

- R1: populated
- R2, R3: not populated
- R4, R5 (feedback resistors): populated if needed to obtain appropriate voltage per the updated PCH VID encoding table above. Consult with VR vendor for appropriate values

For VRs that only support up to 0.95V natively with VID options, using R4 and R5 to shift the voltage table up 50mV will result in the LPM voltage output being shifted up slightly. If the VR supports LPM voltage, the specified, lowest supportable voltage is 0.70V for optimized power consumption. With R4, R5 configured to shift from 0.95V to 1.00V, the LPM voltage will effectively be shifted from 0.70V to ~0.75V. This will not be a functional issue for the platforms, but will slightly de-optimize power consumption. It is recommended that customers work with their VR vendors to adjust to the new voltage table.

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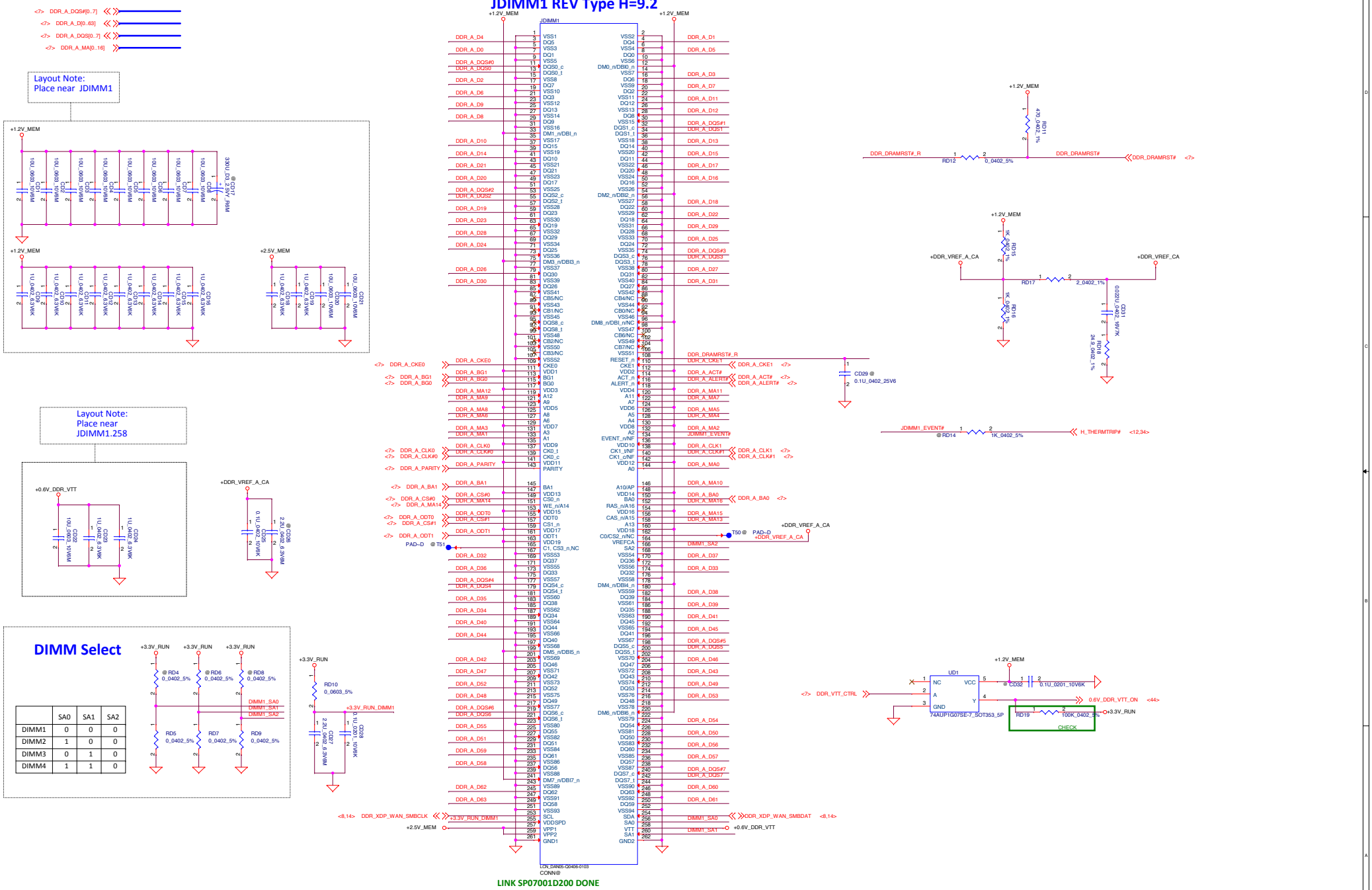
For DDR4

JDIMM1 REV Type H=9.2



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Compal Electronics, Inc.

Title: DDR4

Size: | Document Number: LA-E121P | Rev: 0.1

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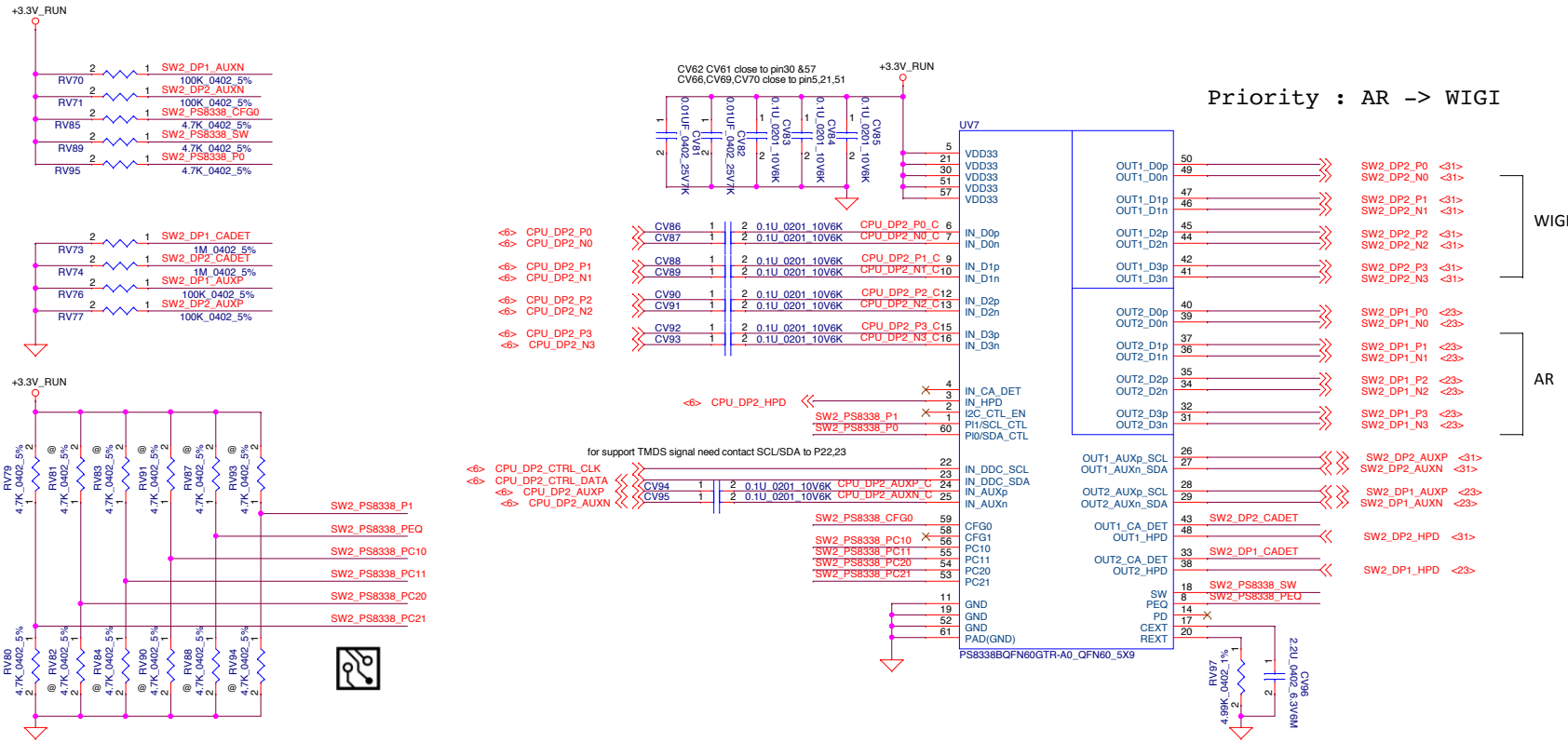
For Steamboat12/14 &Kirkwood



Port switching control or priority configuration. Internal pull down ~150KΩ, 3.3V I/O
For Control Switching Mode (CFG0 = L):
SW = L: Port1 is selected (default)
SW = H: Port2 is selected
For Automatic Switching Mode (CFG0 = H):
SW = L: Port1 has higher priority when both ports are plugged
SW = H: Port2 has higher priority when both ports are plugged (default)

vender suggest MUX use LLEQ PEQ=M and PI0=H !!

Programmable input equalization levels, Internal pull down at ~150Kohm,3.3V I/O
PEQ =
L: default,LEQ, compensate channel loss up to 11.5dB @HBR2
H: HEQ, compensate channel loss up to 14.5dB @HBR2
M:LLEQ, compensate channel loss up to 8.5dB @HBR2

PI0:Automatic EQ disable, Internal pull down ~150K ohm, 3.3V I/O
PI0 = L: Automatic EQ enable(default)
H: Automatic EQ disable

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Compal Electronics, Inc.

Title: DP SW2 PS8338

Size | Document Number: LA-E121P | Rev: 0.1

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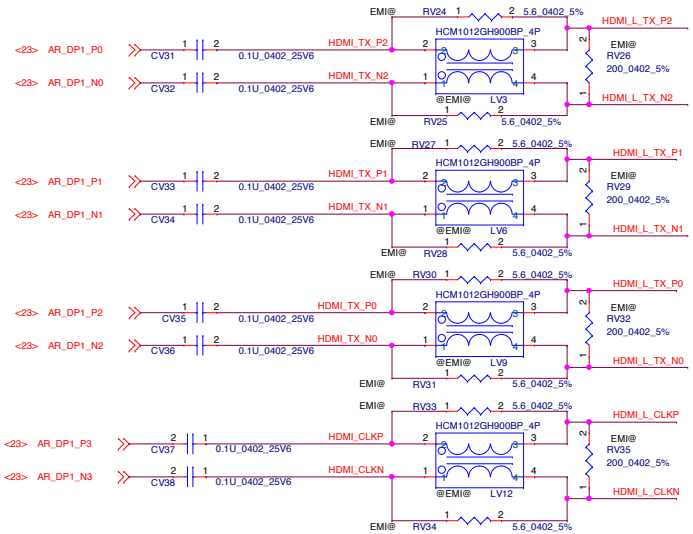
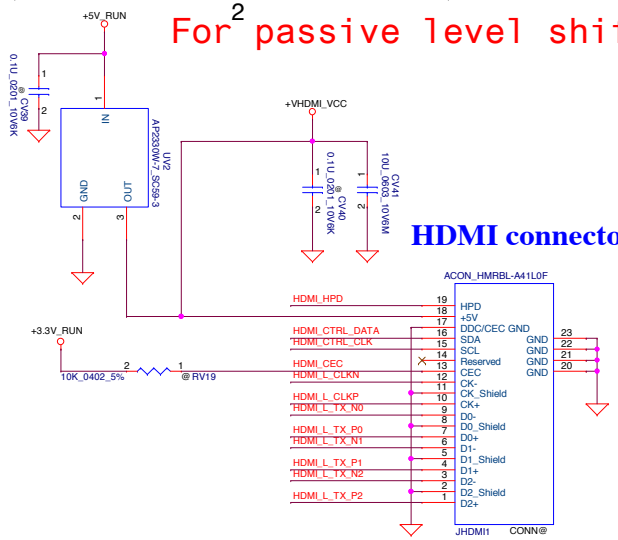
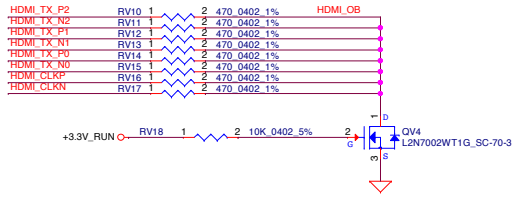
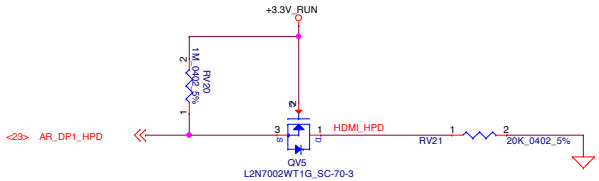
For passive level shifter from AR

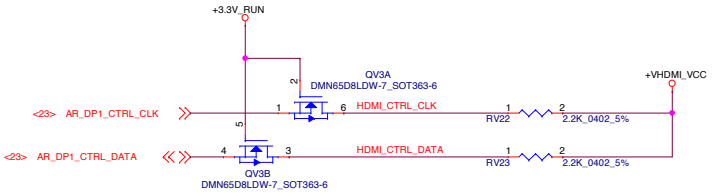




LINK DC231604012 (temp) DONE







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Compal Electronics, Inc.

Title: HDMI CONN

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For Steamboat 12/14

CPU

PS8338

Type C

Close UT1
Intel Review request
20160324

Intel review request
20160324

PI3WVR31313A has internal PD 120Kohm

PI3WVR31310 has internal PD 120Kohm

SNK0_DDC_data/clk – connect to 2k_PU only if SRC0 is connected and support HDMI (a.i HDMI or DP++ connector). Otherwise can be 100k_PD.
SNK1_DDC_data – connect to 100k_PD. If SRC0 support HDMI, connect as SNK0_CFG1 to GPU and/or appropriate AUX/DDC demux control
SNK1_DDC_clk – connect to 100k_PD.

Rework Debug Pin1 +3.3V_TBT_LC, Pin6 GND

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Compal Electronics, Inc.

Title: TBT-AR-SP(1/2) DP, PCIE

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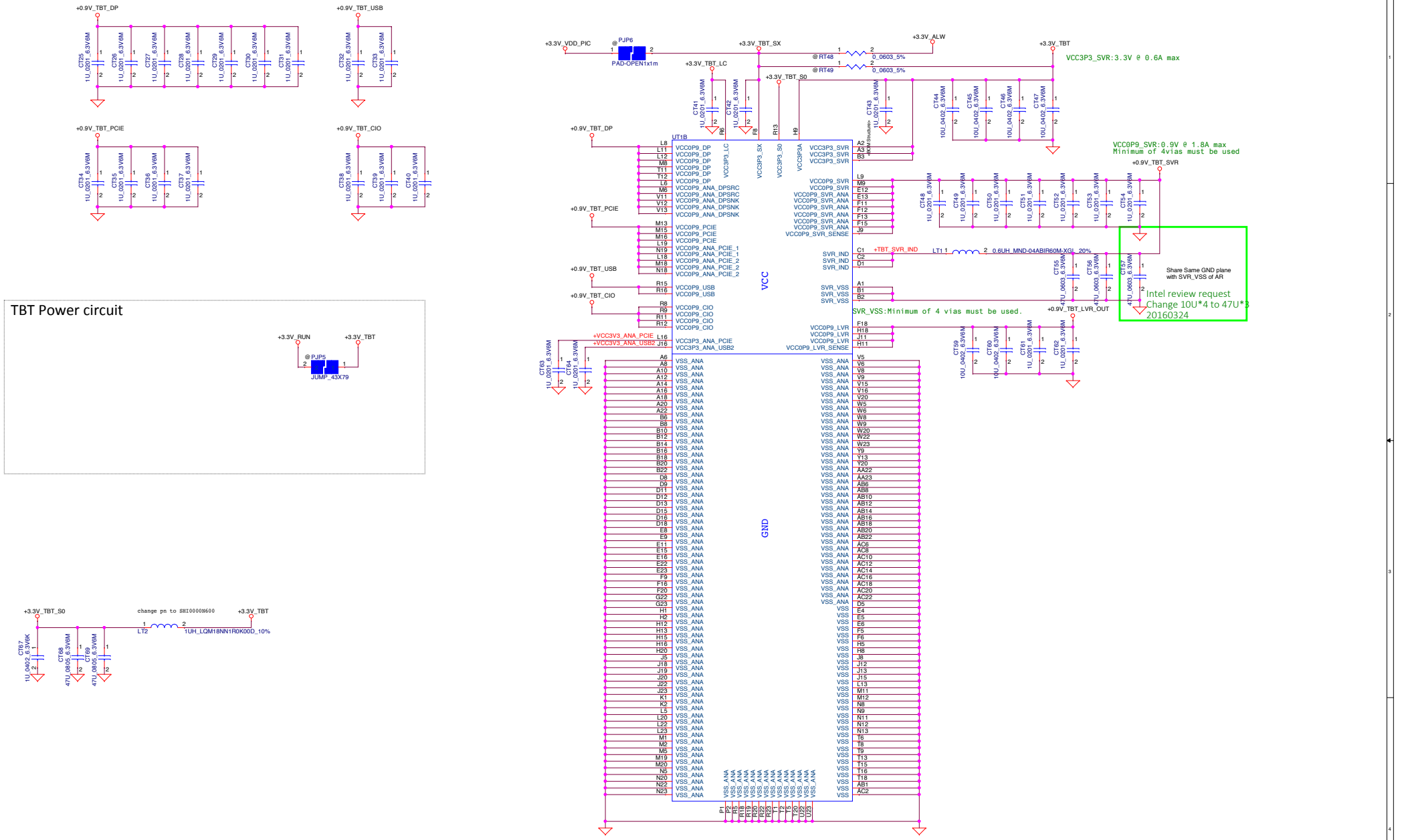
For Steamboat 12/14 &kirkwood,For AR



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Compal Electronics, Inc.

Title	TBT-AR-SP(2/2) PWR,VSS	
Size	Document Number	Rev
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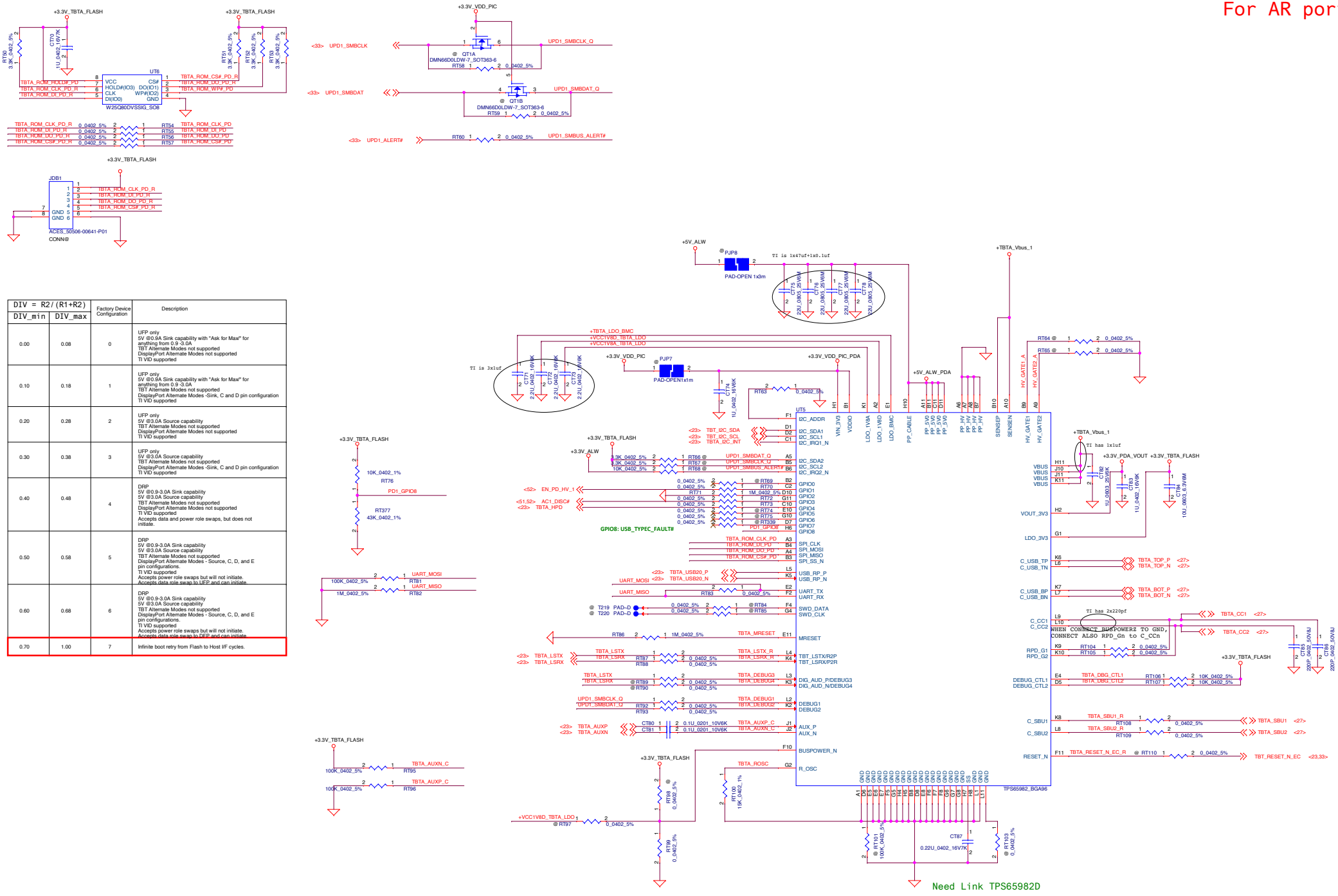
For AR port1



DIV = R2/(R1+R2)		Factory Device Configuration	Description
DIV_min	DIV_max		
0.00	0.08	0	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.10	0.18	1	UFP only 5V @0.9A Sink capability with "Ask for Max" for anything from 0.9 -3.0A TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.20	0.28	2	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported
0.30	0.38	3	UFP only 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes -Sink, C and D pin configuration TI VID supported
0.40	0.48	4	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes not supported TI VID supported Accepts data and power role swaps, but does not initiate.
0.50	0.58	5	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to UFP and can initiate.
0.60	0.68	6	DRP 5V @0.9-3.0A Sink capability 5V @3.0A Source capability TBT Alternate Modes not supported DisplayPort Alternate Modes - Source, C, D, and E pin configurations. TI VID supported Accepts power role swaps but will not initiate. Accepts data role swap to DFP and can initiate.
0.70	1.00	7	Infinite boot retry from Flash to Host I/F cycles.

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Compal Electronics, Inc.

Title: [Type C]PD Controller TI

Size: | Document Number: LA-E121P | Rev: 0.1

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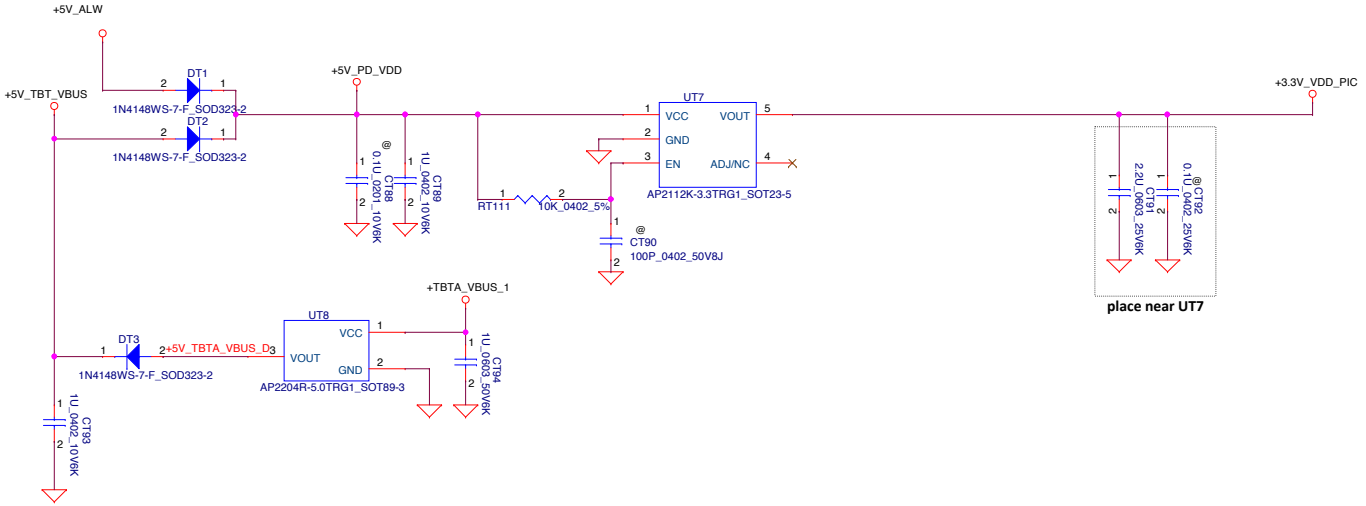

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Compal Electronics, Inc.

Title: [Type C]PD Power

Size | Document Number: LA-E121P | Rev: 0.1

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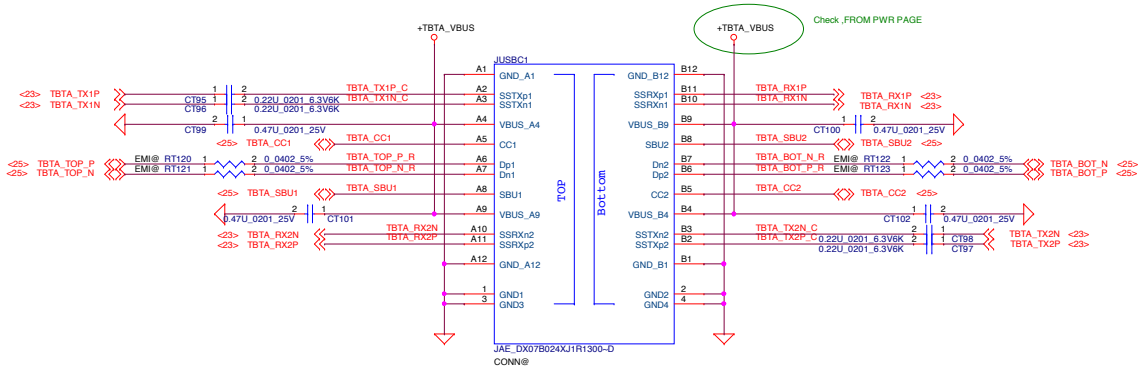
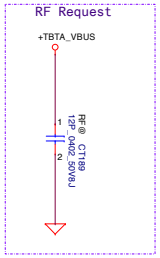
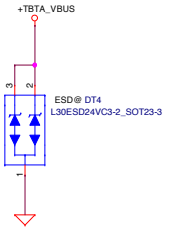
For AR Config

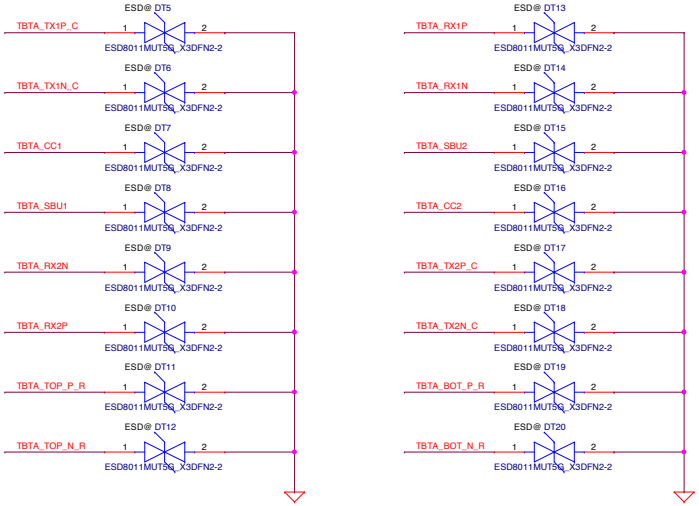


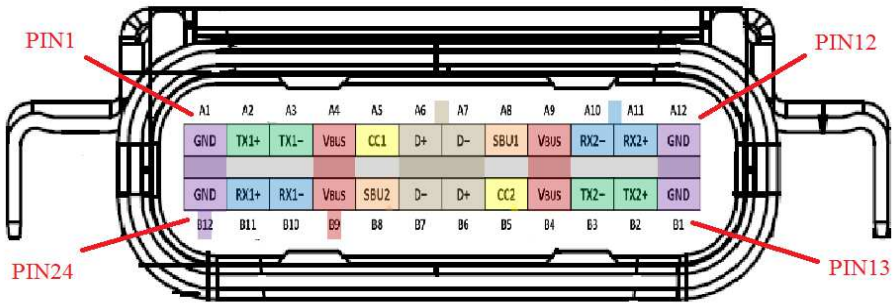
RF Request





Premium 12/14/15 UMA:Check SBU1/SBU2 connect to PD or PS8740B
Link DC23300MEBL Done





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Compal Electronics, Inc.

Title: USB 3.0 CONN TYPE C

Size | Document Number: LA-E121P | Rev: 0.1

Date: Monday, April 25, 2016 | Sheet 27 of 52

LINK 50398-04041-001 DONE

For 2LANE EDP &3.3V_TSP
For Breckenridge&Steamboat 12

JEDP1
ACES_50398-04041-001
CONN@

TOUCH_PANEL_INTR#:
Close lid >> TP_EN = 0 >> Disable touch events
Open lid >> TP_EN = 1 >> Enable touch events

EXC24CQ900U_4P
LV27 EMI@

ESD depop location

EMI Request

Due to SB12/14 Mic. receive path is different between Touch and Non-Touch Panel, so add TOUCH_SCREEN_DET# pin for different verb table

RF Request

Reserve for EA

Close to JEDP1.17~19
Close to JEDP1.30~31
Close to JEDP1.11
Close to JEDP1.1
Close to JEDP1.10

CONN@ JIR1
E-T_4251K-F06N-40L

SB12 : SP01001YO00
SB14 : SP010023D00

DV1 BAT54CW_SOT323-3
DV2 BAT54CW_SOT323-3

For Touchscreen
For Breckenridge 12

QV8 LP2301ALT1G_SOT23-3
QV7 L2N7002WT1G_SC-70-3

WebCAM

QZ1 LP2301ALT1G_SOT23-3
EXC24CQ900U_4P
LZ1 EMI@

Backlight POWER

QV1 AO6405_TSOP6
QV2 L2N7002WT1G_SC-70-3

LCDVDD POWER

UV24 G524B1T11U_SOT23-5
DV3 BAT54CW_SOT323-3

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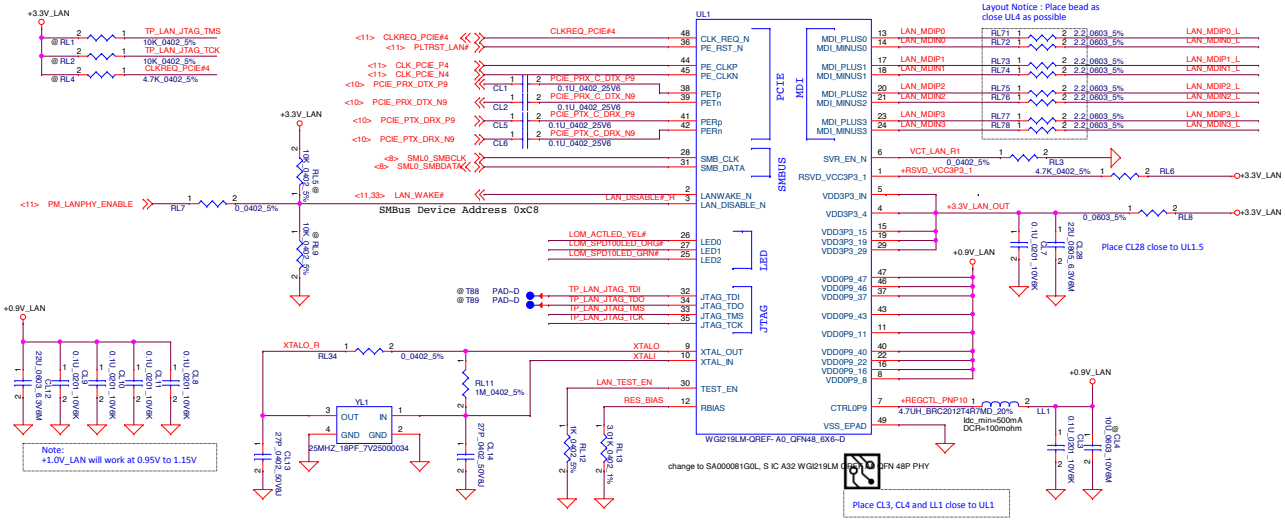
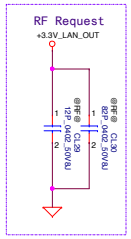
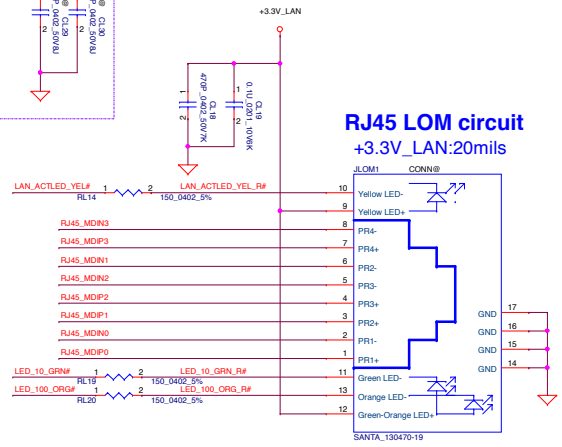
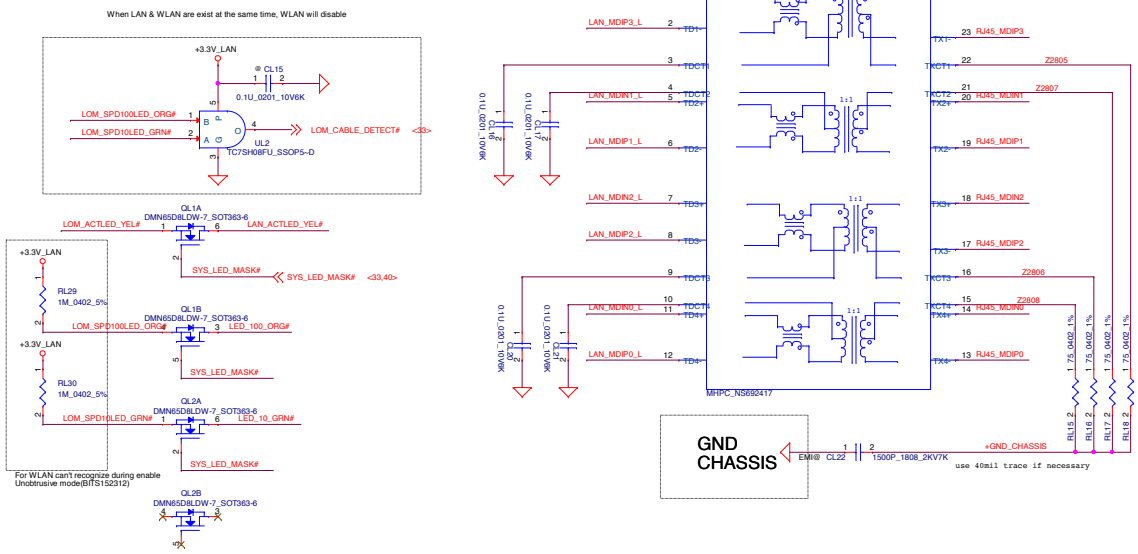
Compal Electronics, Inc.	
Title	eDP CONN & Touch screen
Size	Document Number: LA-E121P
Rev	0.1
Date:	Monday, April 25, 2016
Sheet	28 of 52







Link DC231603220 (temp) DONE



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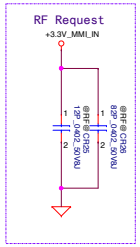
Compal Electronics, Inc.

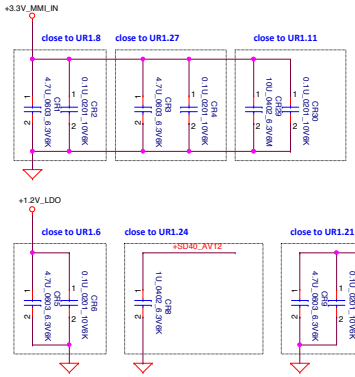
Title: LAN Clarkvillie & RJ45

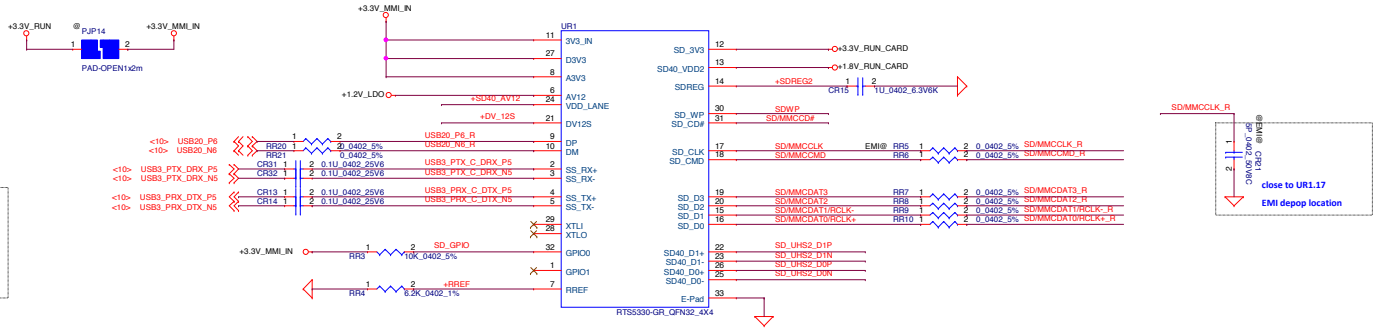
Size | Document Number: LA-E121P | Rev: 0.1

Date: Monday, April 25, 2016 | Sheet 29 of 52

USB INTERFACE,For Steamboat

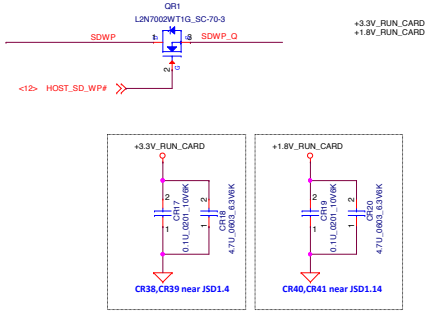


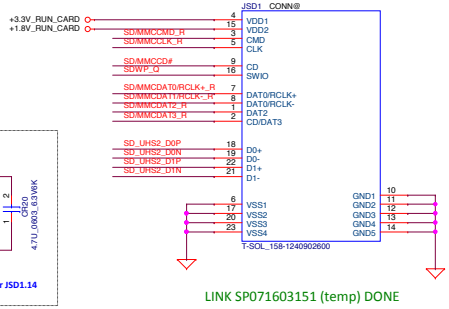




SA00009UH00 Link Done

HOST_SD_WP#	SDWP_Q	SDWP	STATUS
High	High	High	Write Protect(SD LOCK)
	Low	Low	Write Enable
Low	High	High	Write Protect(SD& FW LOCK)
	Low	High	Write Protect(FW LOCK)





LINK SP071603151 (temp) DONE

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Compal Electronics, Inc.

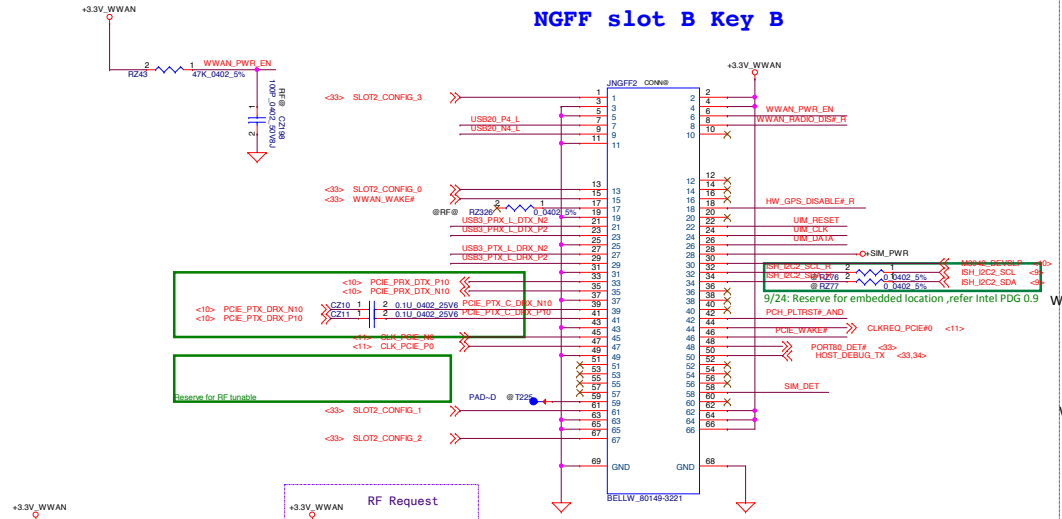
Title: Card Reader RTS5330

Size: | Document Number: LA-E121P | Rev: 0.1

Date: Monday, April 25, 2016 | Sheet 30 of 52

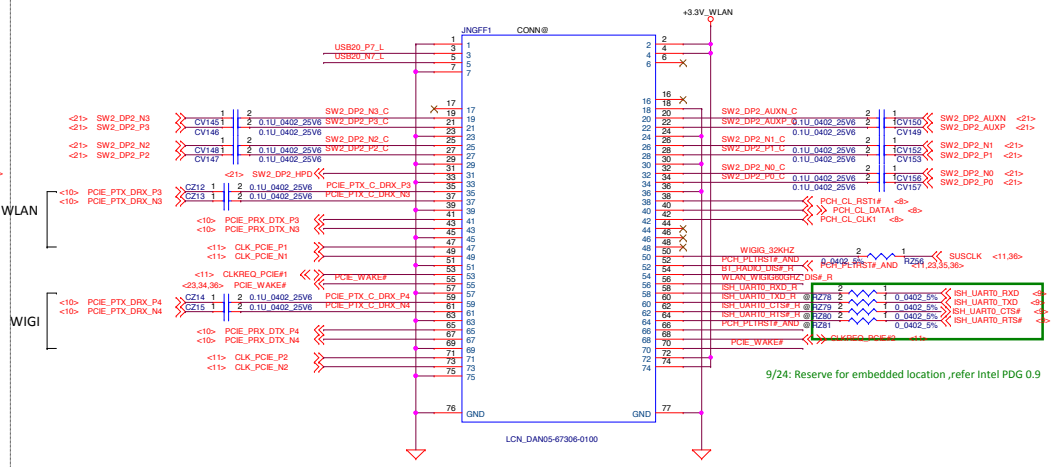
for AR Steamboat

NGFF slot B Key B



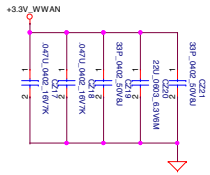
80149-3221 LINK DONE

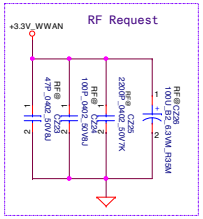
NGFF slot A Key A

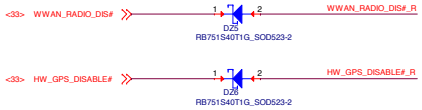


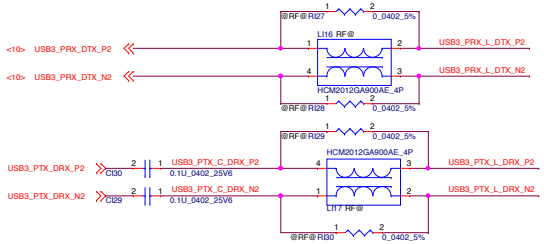
SP070019F00 LINK DONE

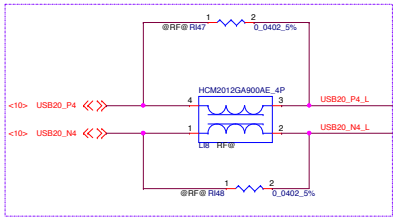
9/24: Reserve for embedded location ,refer Intel PDG 0.9

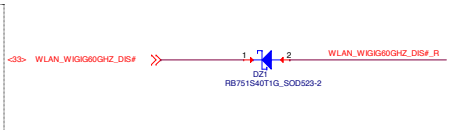


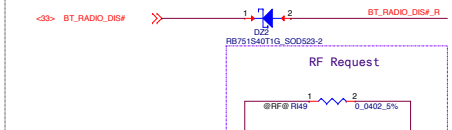


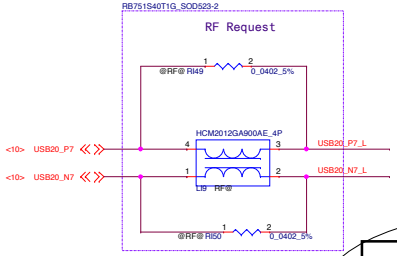


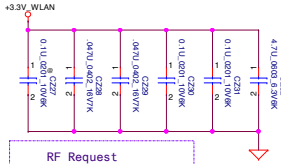


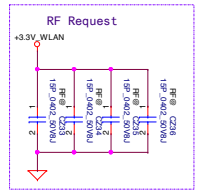




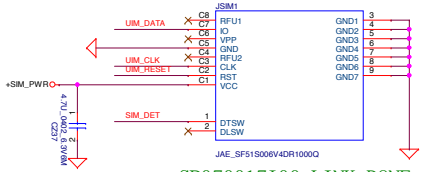




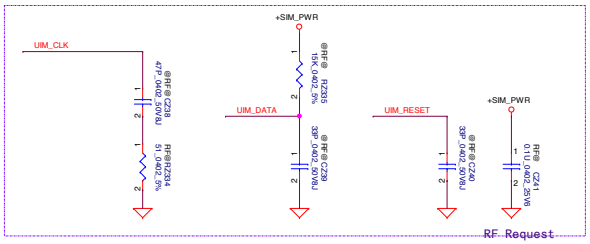




SIM Card Push-Push



SP070017I00 LINK DONE



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE(2 lane)
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE(1 lane)
15	HIGH	HIGH	HIGH	HIGH	NA

Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

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Compal Electronics, Inc.

Title: NGFF Card

Size: | Document Number: LA-E121P | Rev: 0.1

Date: Monday, April 25, 2016 | Sheet 31 of 52

1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

JSPK1 CONN@ — ACES_50278-0040N-001

Link SP02001CE00 DONE

Close to UA1

Close to UA1 pin6

place close to UA1 pin3

Place closely to Pin 13.

Add for solve pop noise and detect issue

place at AGND and DGND plane

CLASS-D POWER DOWN CONTROL CIRCUIT

HDA_Link is 3.3V,no need level shift circuit

RE313@one control line if DVDD is 3.3V
DE2@two control lines1

Power sequence +5V_RUN_AUDIO(501us) > +3.3V_RUN_AUDIO(1204 us) > +1.5V_RUN

Reserve for support D3 cold

2.5A

500mA

UA1 — ALC3246-CG_MQFN48_6X6

Place CA29 close to Codec

SLEEVE/RING2 please keep 40 mils trace width

AUD_HP_OUT_L/ AUD_HP_OUT_Rplease keep 15 mils trace width

Add this Filter to avoid other components/chips be influenced

HP-Out-Right
HP-Out-Left
Nokia-MIC
iPhone-MIC

Global Headset
Universal Jack

Normal
Open

Only BR15U UMA use LA2,LA3,because 6L

JHP1 CONN@ — SINGA_2SJ3095-085111F

Link DC23000DG10 DONE

RF Request

DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2016/01/01	Deciphered Date	2017/01/01

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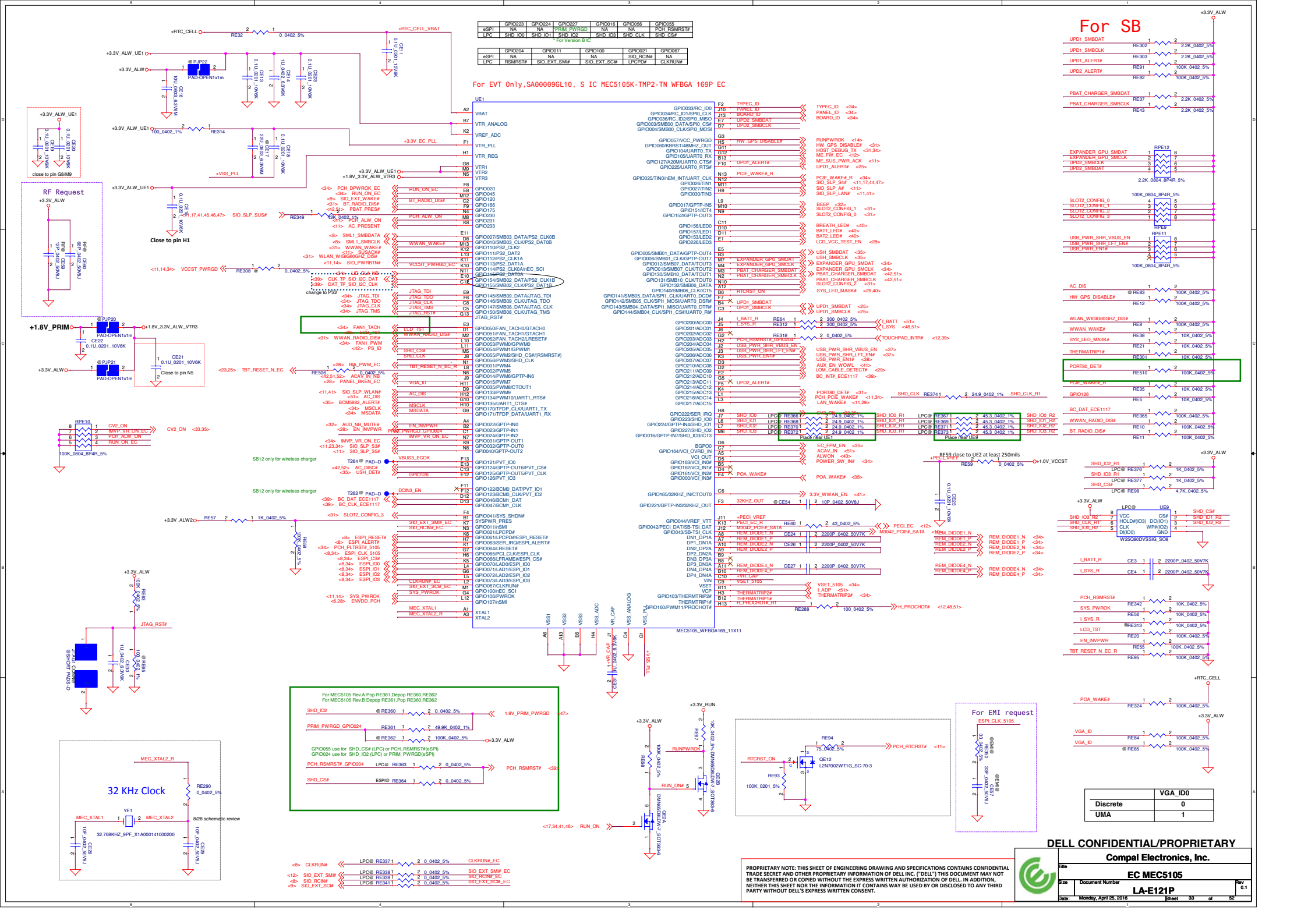
Compal Electronics, Inc.

Title: Codec ALC3246

Size: C | Document Number: LA-E121P | Rev: 0.1

Date: Monday, April 25, 2016 | Sheet 32 of 52



	GPIO223	GPIO224	GPIO227	GPIO016	GPIO056	GPIO055
eSPI	NA	NA	*PRIM_PWRGD	NA	NA	PCH_RSMRST#
LPC	SHD_IO0	SHD_IO1	SHD_IO2	SHD_IO3	SHD_CLK	SHD_CS#

* For Version B IC

	GPIO204	GPIO011	GPIO100	GPIO021	GPIO067
eSPI	NA	NA	NA	SIO_RCIN#	NA
LPC	RSMRST#	SIO_EXT_SMI#	SIO_EXT_SCI#	LPCPD#	CLKRUN#

	VGA_ID0
Discrete	0
UMA	1

Date:	Monday, April 25, 2016
Sheet	33 of 52

For SB

PAGE	ESPI	LPC
8	RC25_10K	RC8_15ohm RC13/RC27_8.2K
18	RC212_0ohm 0603	RC211_0ohm 0603
31		RE337,RE338 RE339,RE340, RE341 0_ohm
32	RE2 / RE3 0_ohm	

LPC 80Port Debug	LPC	ESPI
1	+3.3V_RUN	+3.3V_RUN
2	+3.3V_RUN	+3.3V_RUN
3	LPC_LAD0	ESPI_IO0
4	LPC_LAD1	ESPI_IO1
5	LPC_LAD2	ESPI_IO2
6	LPC_LAD3	ESPI_IO3
7	LPC_FRAME#	ESPI_CS#
8	PCH_PLTRST#	NA
9	GND	GND
10	LPC_CLOCK	ESPI_CLK

RE343	CE62	REV
240K	4700p	Single Port ACE w/o AR
130K	4700p	Single Port ACE w/AR
62K	4700p	Dual Port ACE w/o AR
33K	4700p	Dual Port ACE w/AR
8.2K	4700p	Dual Port ACE (w/AR +w/o AR)
4.3K	4700p	.
2K	4700p	
1K	4700p	

PD_ACE_DET# rise time is measured from 5%~68%.

RE79	CE40	REV
240K	4700p	X00
130K	4700p	
62K	4700p	
33K	4700p	
8.2K	4700p	
4.3K	4700p	
2K	4700p	
1K	4700p	

BOARD_ID rise time is measured from 5%~68%.

RE300	CE47	PANEL SIZE
240K	4700p	12"
130K	4700p	14"
33K	4700p	15"
4.3K	4700p	17"

PANEL_ID rise time is measured from 5%~68%.

Reset Threshold Level 3.0V

CT: 3300 pF ~ 10ms delay

Rest=1.58K , Tp=96 degree???

Link 50271-0040N-001 DONE

Thermal diode mapping

5105 Channel	Location
DP1/DN1	CPU (QE3)
DP2/DN2	WiGig (QE5)
DP2a/DP2a	DDR (QE7)
DP3/DN3	NA
DP4/DN4	CPU VR (QE6)

Place under CPU
Place CE35 close to the QE3 as possible

DP2/DN2 for WiGig on QE5, place QE5 close to WiGig and CE37 close to QE5

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

DN2a/DP2a for DDR on QE7, place QE7 close to DDR and CE46 close to QE7

Control Byte

0	1	0	0	A2	A1	A0	R/W

R/W = 0 = Wire
R/W = 1 = Read

SMBus address 0x40

Link ITE IT8010 SA00009VL00 OK

CHECK

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Title: MEC5105 support
Size: Document Number: LA-E121P
Rev: 0.1
Date: Monday, April 25, 2016
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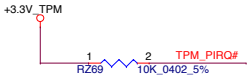
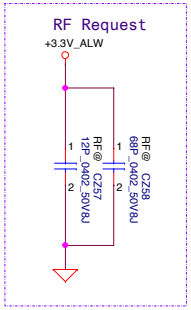
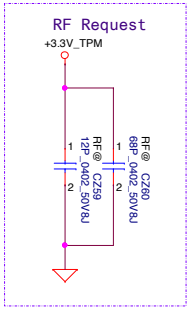
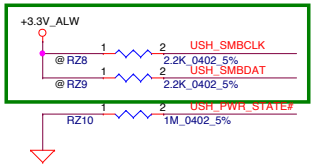
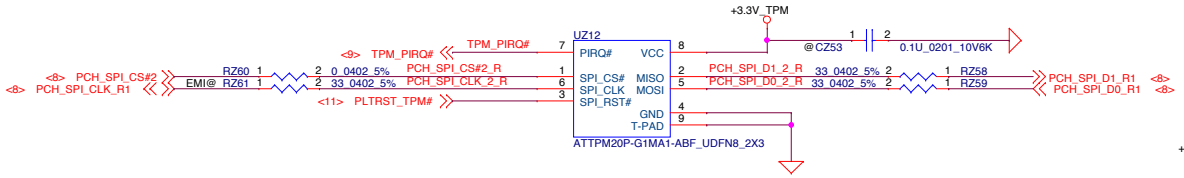
For ATMEL TPM

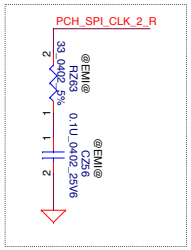




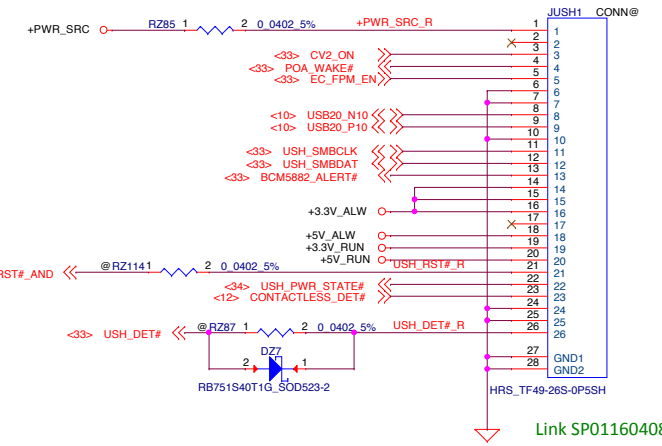




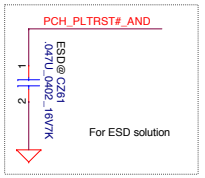




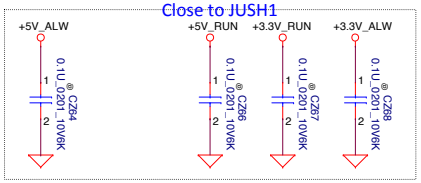
USH CONN

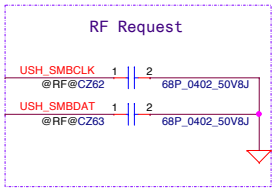


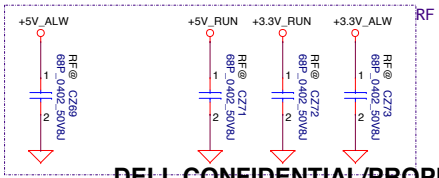
Link SP011604080(temp) DONE



Close to JUSH1







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Compal Electronics, Inc.	
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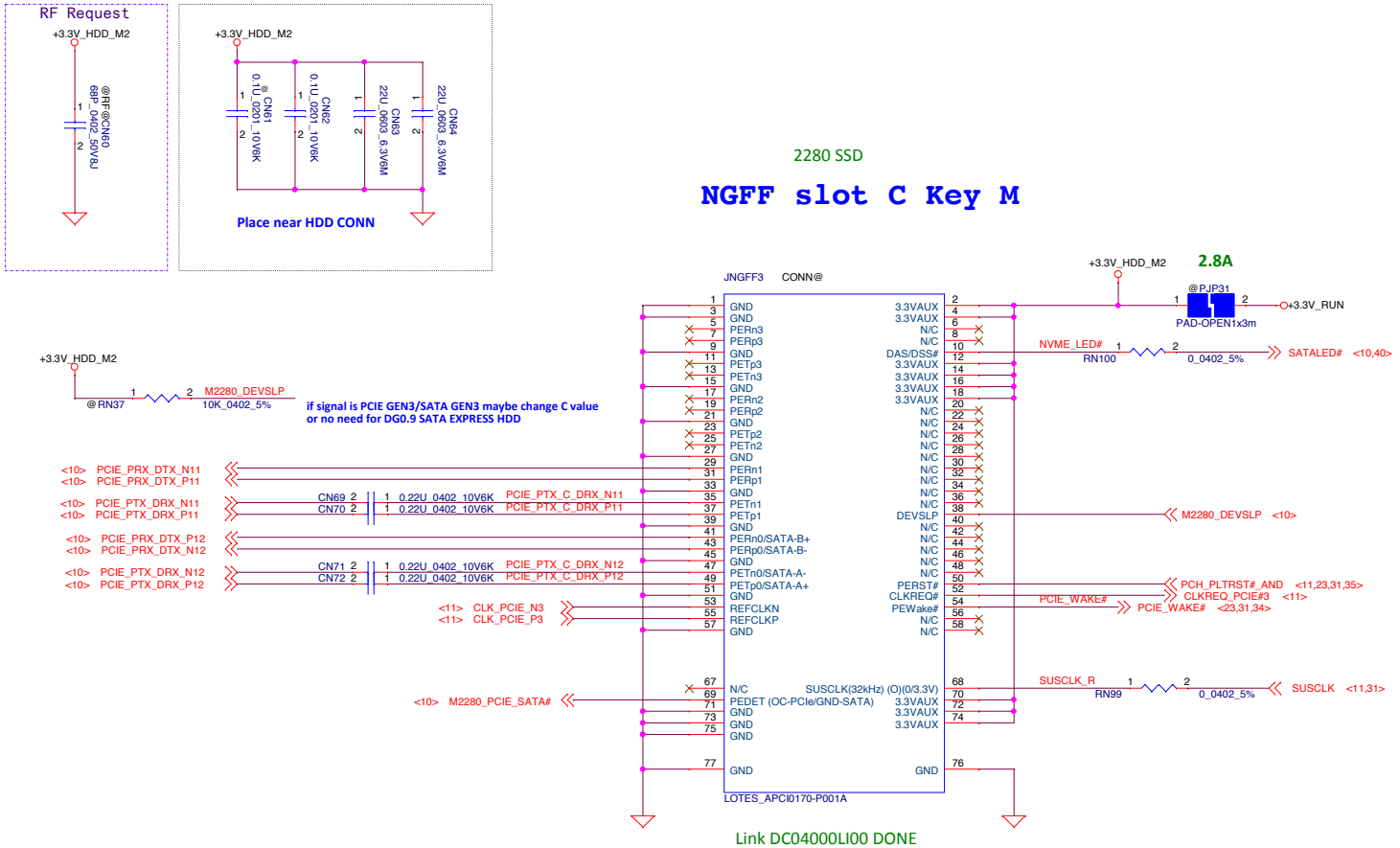
For Brekenridge 12/14/15 UMA/Steamboat



Link DC04000LI00 DONE

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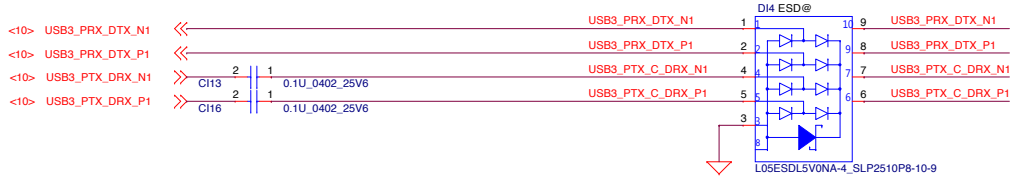
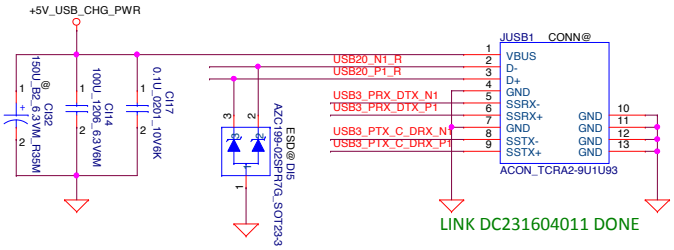
Compal Electronics, Inc.

Title: M2 2280 Socket

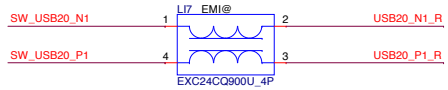
Size | Document Number: LA-E121P | Rev: 0.1

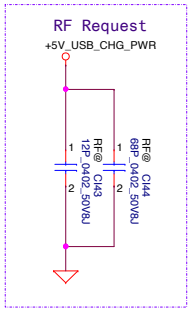
Date: Monday, April 25, 2016 | Sheet 36 of 52

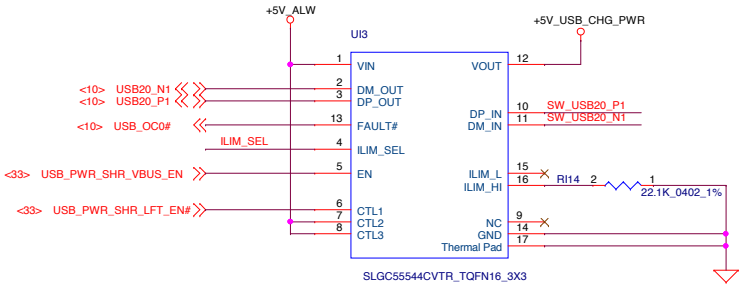




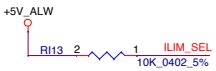
LINK DC231604011 DONE

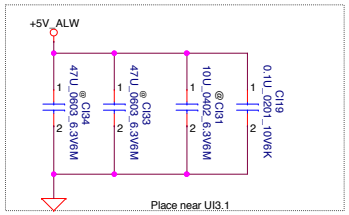






SA000097E10 Link Done





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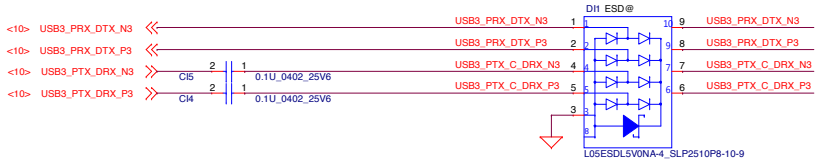
Compal Electronics, Inc.

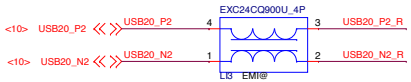
Title: JUSB1+PS

Size | Document Number: LA-E121P | Rev: 0.1

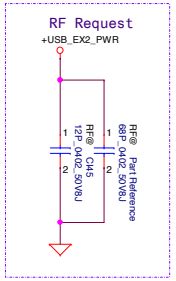
Date: Monday, April 25, 2016 | Sheet 37 of 52

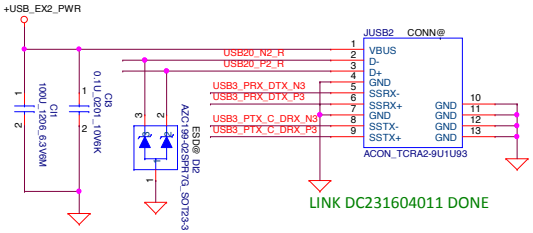
For Breckenridge/Steamboat 12&Kirkwood

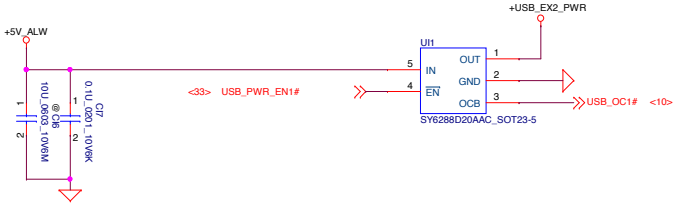




DFB request:
main SM070003Z00 (INPAQ_MCM1012B900F06BP_4P)
Footprint use 2nd source SM070004400 (PANAS_EXC24CQ900U_4P)
Pitch change from 0.5mm to 0.55mm







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Compal Electronics, Inc.

Title	JUSB2	
Size	Document Number LA-E121P	Rev 0.1
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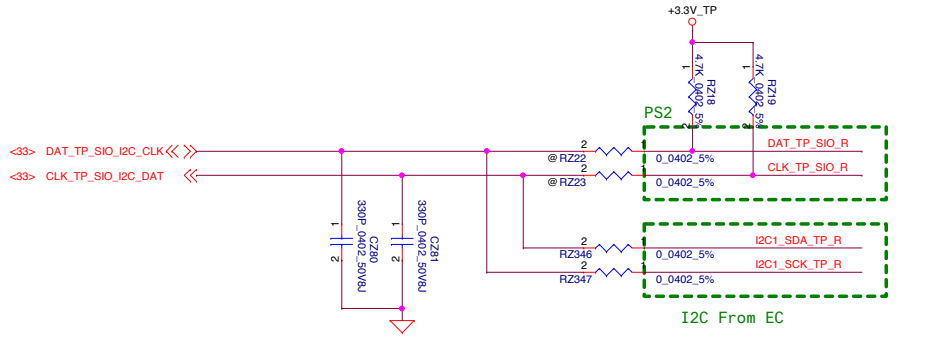
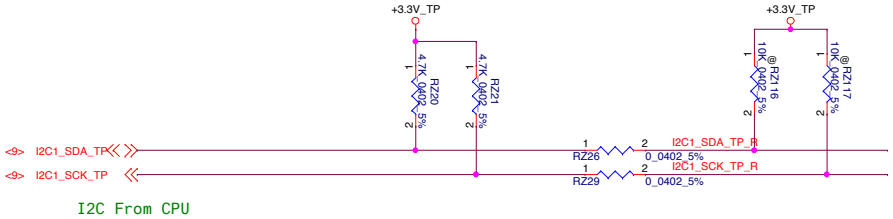
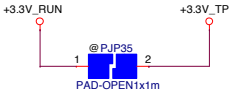
Touch Pad

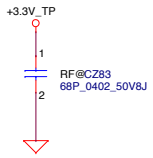




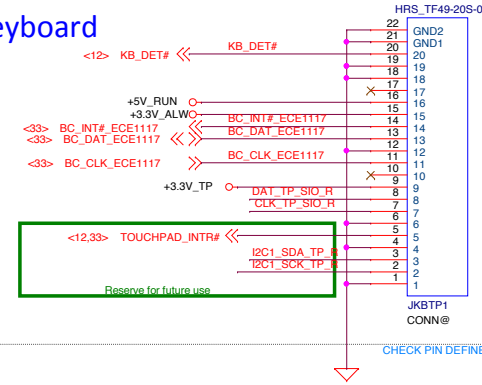
Plan is for I2C to be driven by the EC for Win7 and Pre-OS (will utilize Intel I2C drivers for Win7)
For Win8.1 and 10 the EC will control TP over I2C Pre-OS and then the PCH will drive I2C when in Windows
Route PS2 from EC to the touch pad also for contingency plan if I2C has issues

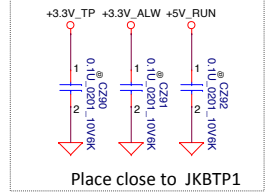


RF Request



Keyboard





Link SP011604085(temp) DONE

@EDP Cable nonTS_HD/FHD-HD Cam

Part Number	Description
DC02C00E000	H-CONN SET 1S5 MB-LCD-CAMERA NTS FHD

@EDP Cable nonTS_FHD-IR

Part Number	Description
DC02C00E100	H-CONN SET 1S5 MB-LCD-CAMERA-IR NTS FHD

@EDP Cable TS_TS-FHD-HD Cam

Part Number	Description
DC02C00E200	H-CONN SET 1S5 MB-LCD-CAMERA-TS FHD

@LED Cable

Part Number	Description
DC02002LT00	H-CONN SET 1S5 MB-LED/B

@FP FFC

Part Number	Description
NBX00023000	FFC 12P F P0.5 PAD=0.3 56MM MB-FP 1S5

@TP FFC

Part Number	Description
NBX00022Y00	FFC 20P F P0.5 PAD=0.3 92MM MB-TP 1S5

@USH Board FFC

Part Number	Description
NBX00022Z00	FFC 26P F P0.5 PAD=0.3 81.6MM MB-USH 1S5

@RTC BATT

Part Number	Description
GC02001DS00	BATT CR2032 3V 225MAH PA 5 W/C 30MM

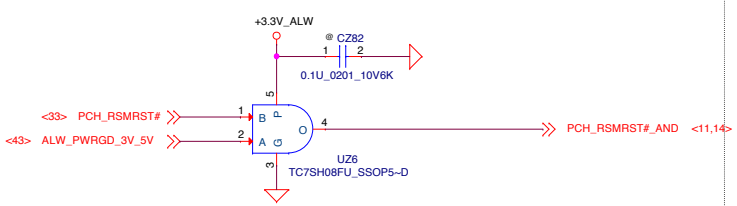
@FAN

Part Number	Description
DC28A000800	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

RSMRST circuit



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Compal Electronics, Inc.

Title: Keyboard

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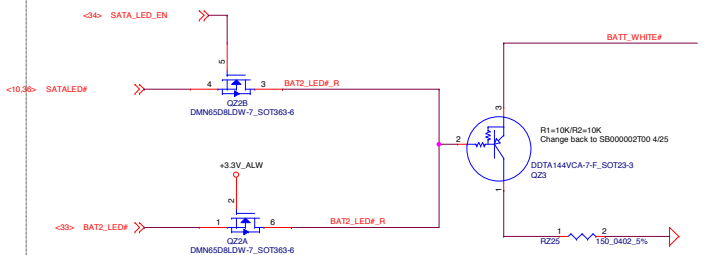
HDD LED MUX

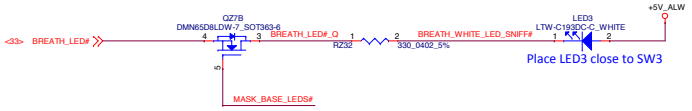
means EC can switch battery white led and HDD LED by hot key "Fn+H"

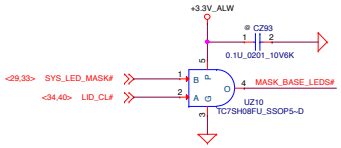


Battery LED

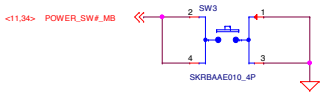
Breath LED

LED P/N change to SCS0000FL00 from SCS0000BA00

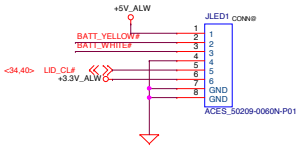




POWER & INSTANT ON SWITCH



LED board CONN

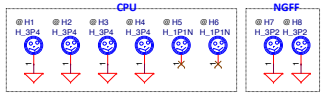


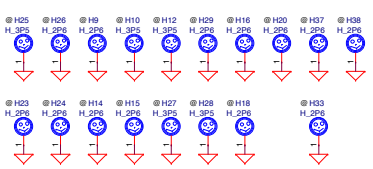
Fiducial Mark

@ FD1 FIDUCIAL MARK~D
@ FD2 FIDUCIAL MARK~D
@ FD3 FIDUCIAL MARK~D
@ FD4 FIDUCIAL MARK~D

LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Unobtrusive mode)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1





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Compal Electronics, Inc.

Title: PAD, LED

Size: | Document Number: LA-E121P | Rev: 0.1

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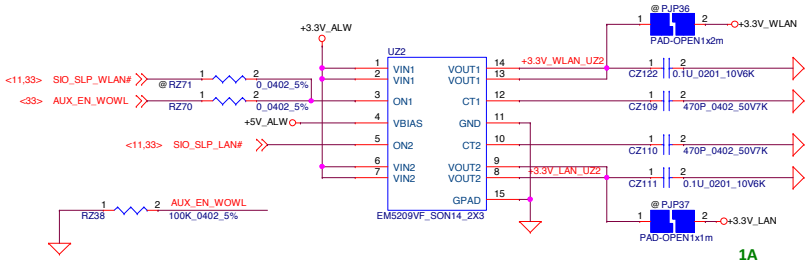
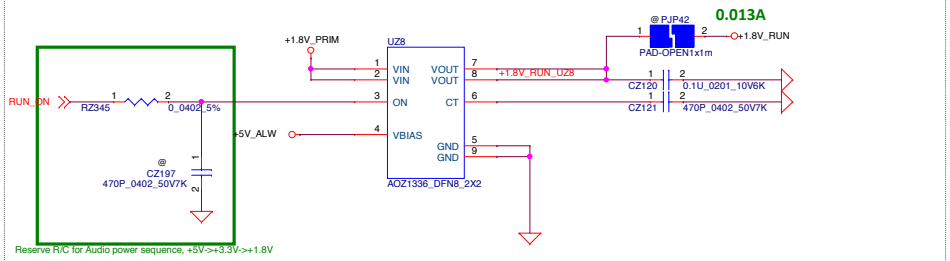
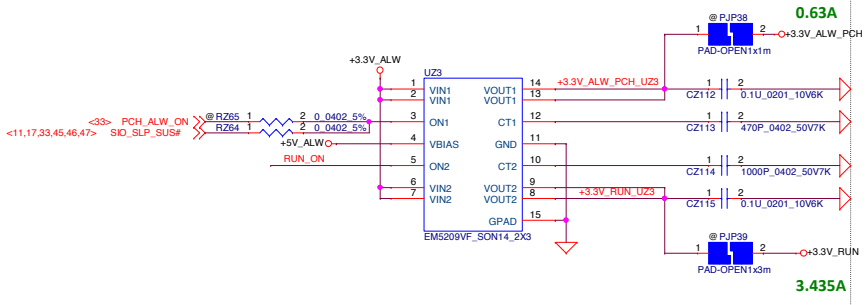
+3.3V_WLAN/+3.3V_LAN source



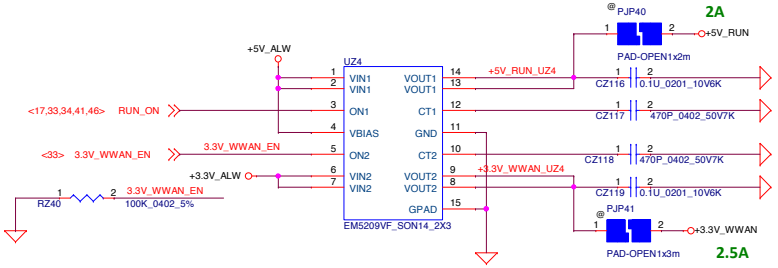
+1.8V_RUN source

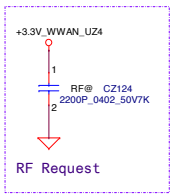


+3.3V_ALW_PCH/+3.3V_RUN source



+5V_RUN/+3.3V_WWAN source





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Compal Electronics, Inc.		
Title: Power control		
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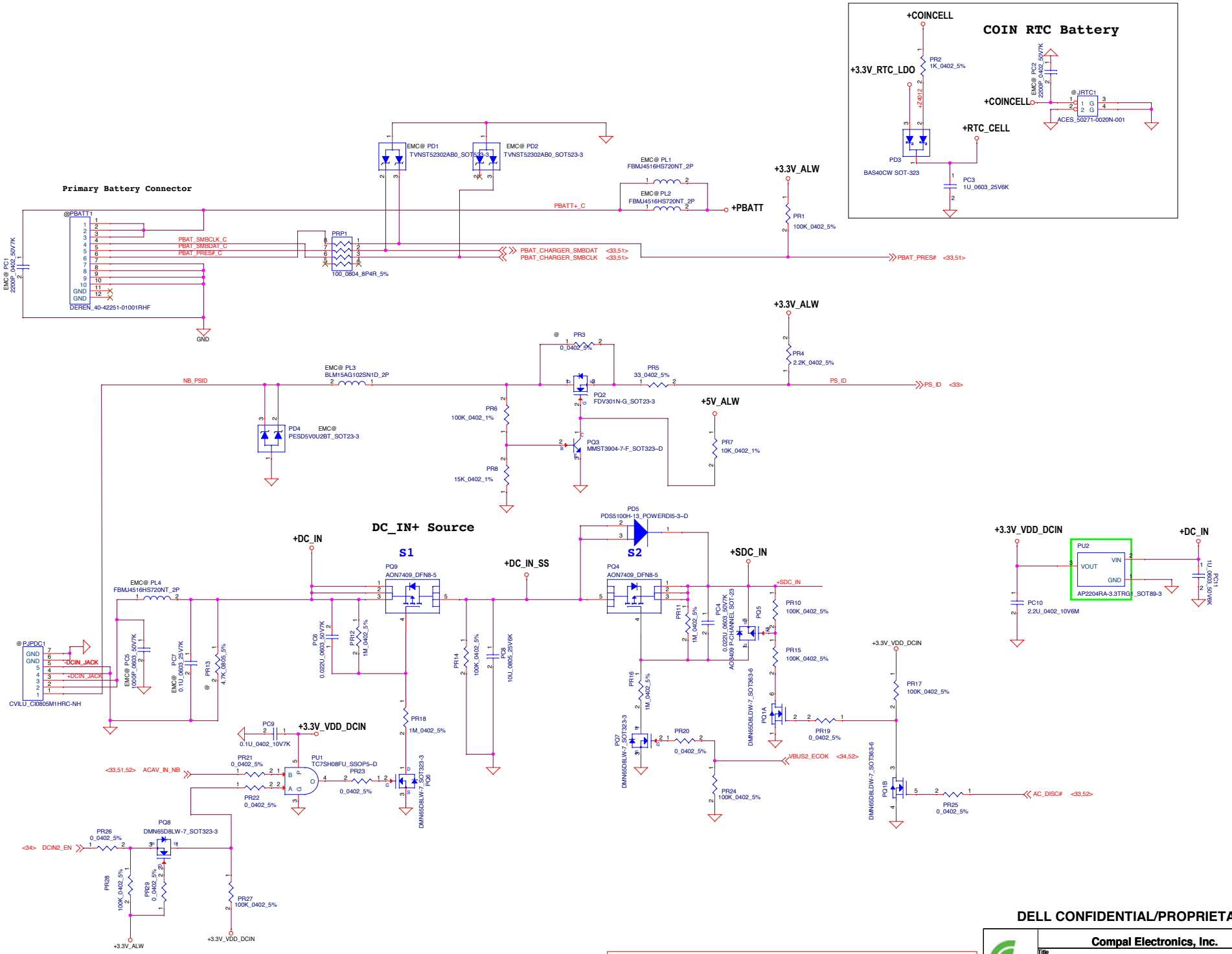

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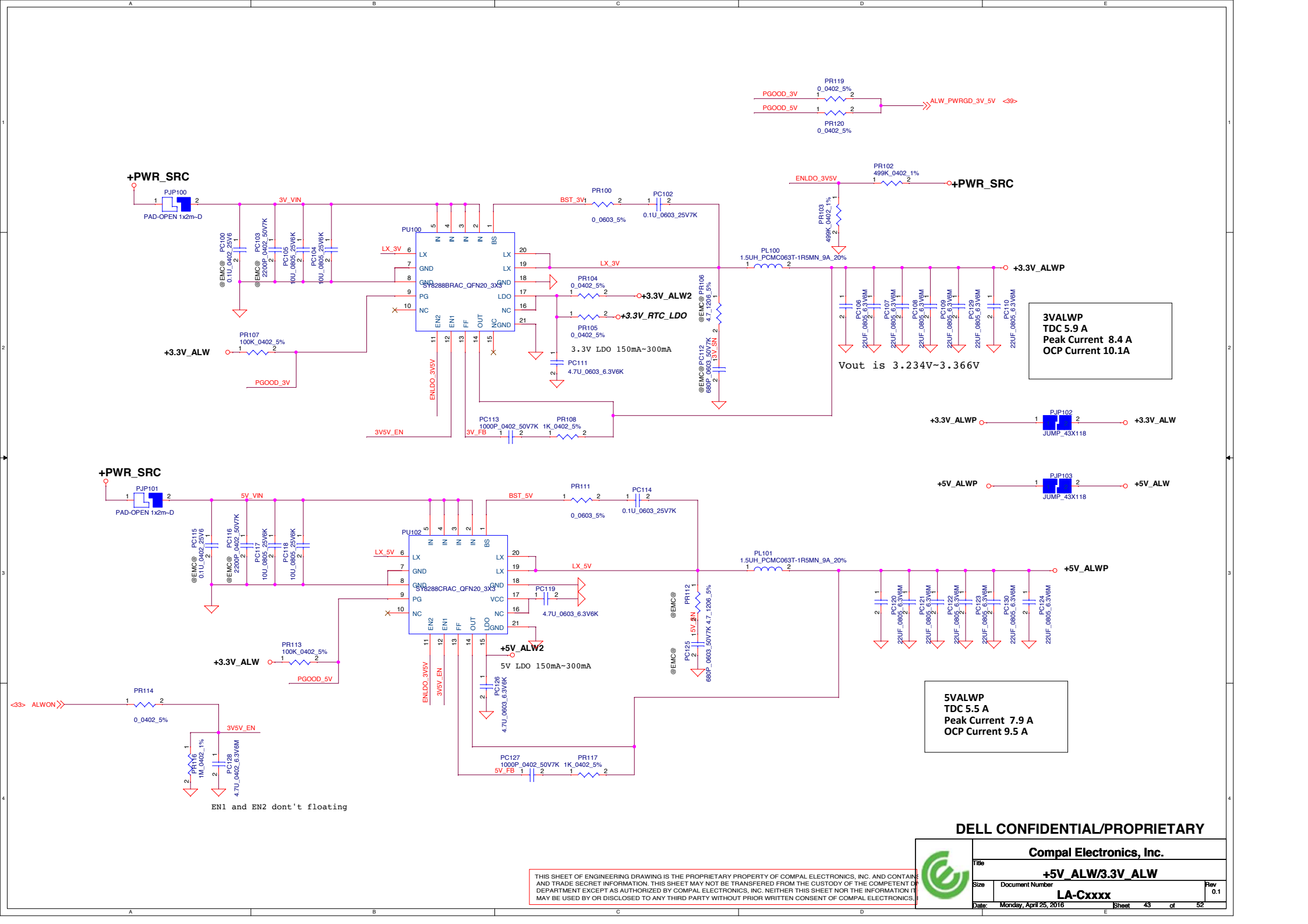
Compal Electronics, Inc.		
Title: +DCIN		
Size	Document Number: LA-Cxxxx	Rev: 0.1
Date: Monday, April 25, 2016	Sheet 42 of 52	



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Compal Electronics, Inc.

Title: +5V_ALW/3.3V_ALW

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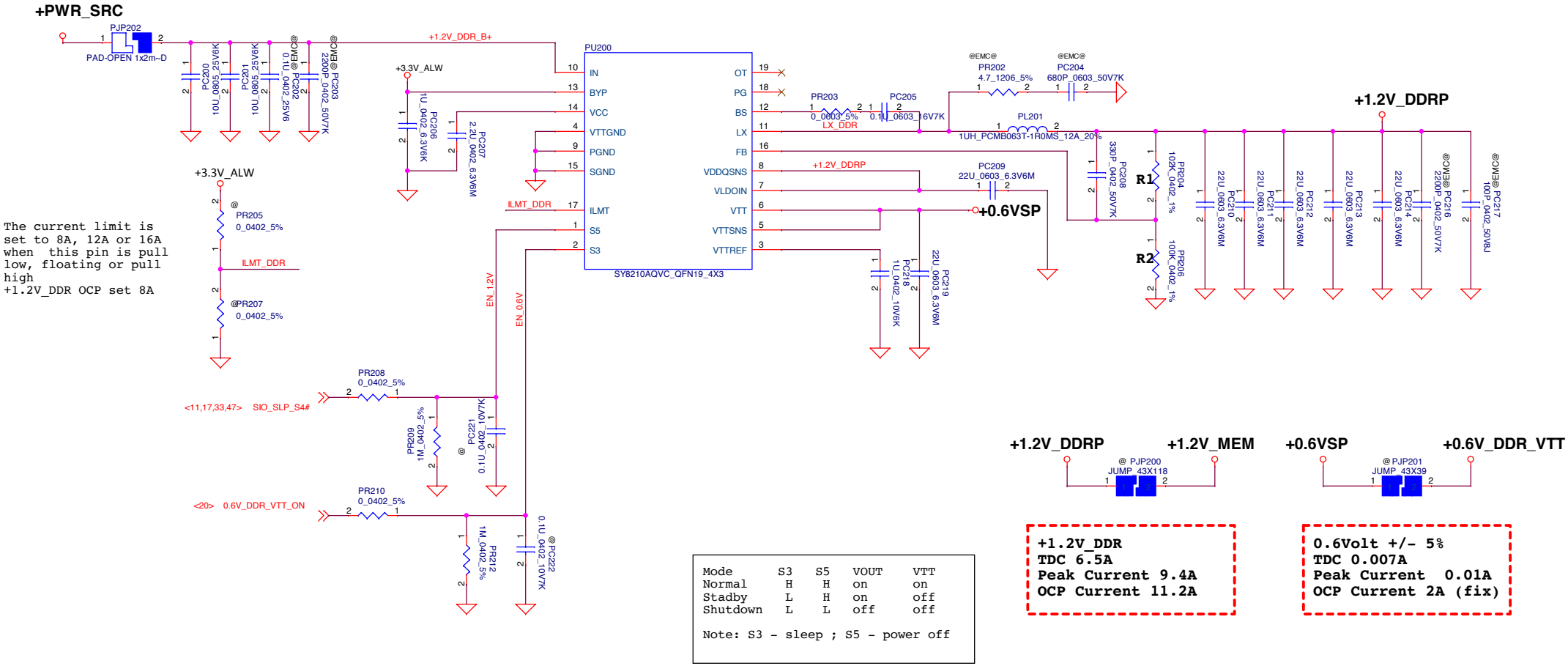

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high
+1.2V_DDR OCP set 8A

Mode	S3	S5	VOUT	VTT
Normal	H	H	on	on
Stadby	L	H	on	off
Shutdown	L	L	off	off

Note: S3 - sleep ; S5 - power off

+1.2V_DDR
TDC 6.5A
Peak Current 9.4A
OCP Current 11.2A

0.6Volt +/- 5%
TDC 0.007A
Peak Current 0.01A
OCP Current 2A (fix)

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Title: +1.2V_MEN/+0.6V_DDR_VTT

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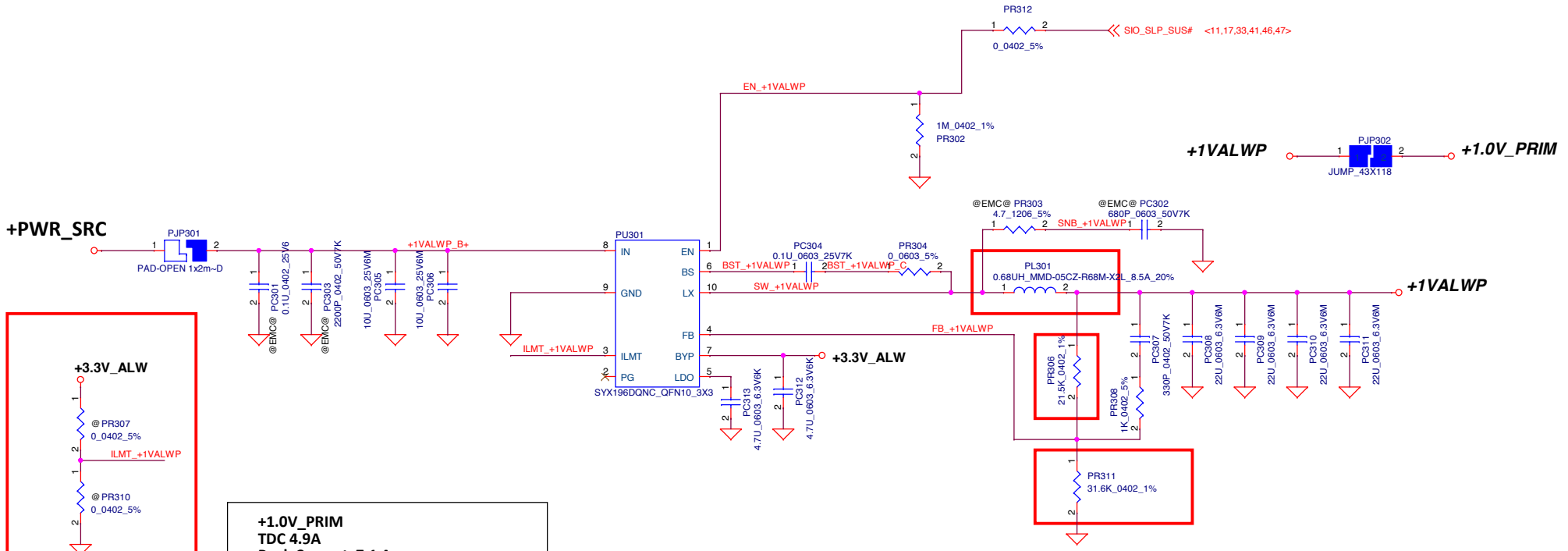

+1.0V_PRIM
TDC 4.9A
Peak Current 7.1 A
OCP Current 8.6A

	TYP	MAX
Choke DCR	11.0mohm ,	12.0mohm

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high

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Title	+1VALWP	
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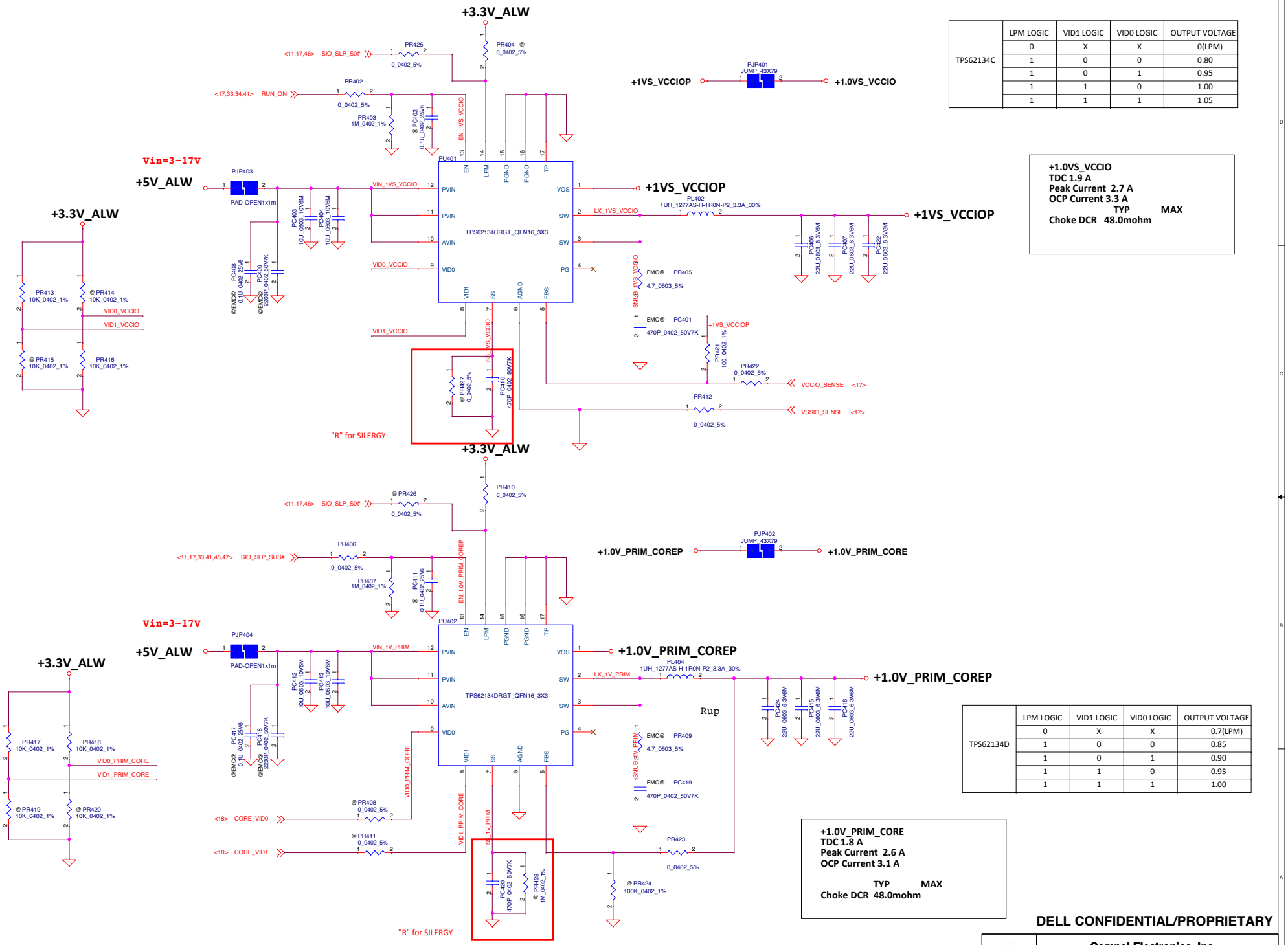

TPS62134C	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0(LPM)
	1	0	0	0.80
	1	0	1	0.95
	1	1	0	1.00
	1	1	1	1.05

+1.0VS_VCCIO
TDC 1.9 A
Peak Current 2.7 A
OCP Current 3.3 A

	TYP	MAX
Choke DCR	48.0mohm	

TPS62134D	LPM LOGIC	VID1 LOGIC	VID0 LOGIC	OUTPUT VOLTAGE
	0	X	X	0.7(LPM)
	1	0	0	0.85
	1	0	1	0.90
	1	1	0	0.95
	1	1	1	1.00

+1.0V_PRIM_CORE
TDC 1.8 A
Peak Current 2.6 A
OCP Current 3.1 A

	TYP	MAX
Choke DCR	48.0mohm	

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Title: +1VS_VCCIOP/+1.0V_PRIM_COREP

Size: | Document Number: LA-Cxxxx | Rev: 0.1

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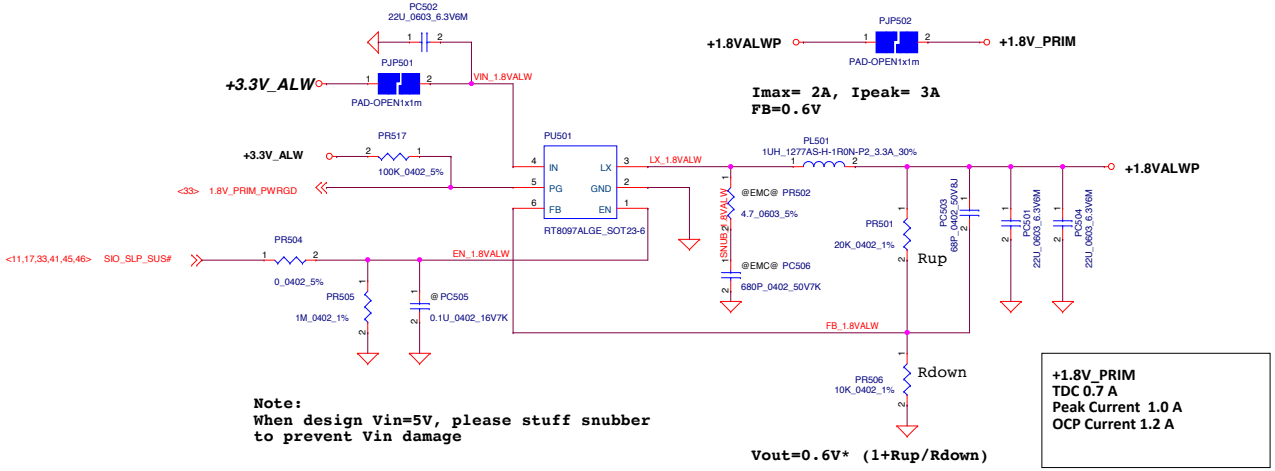

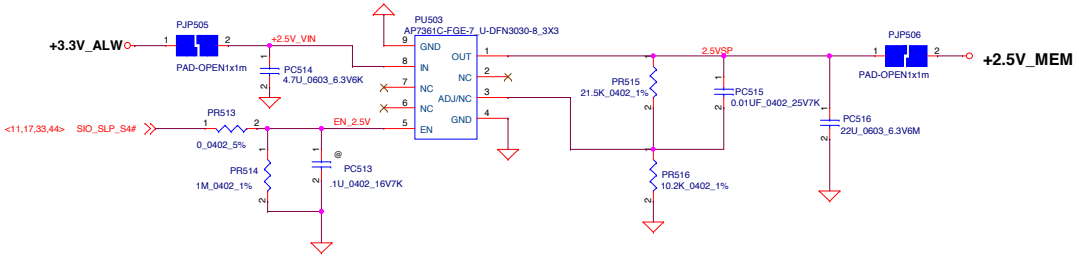

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Title: +1.8VALWP/+1.5VSP

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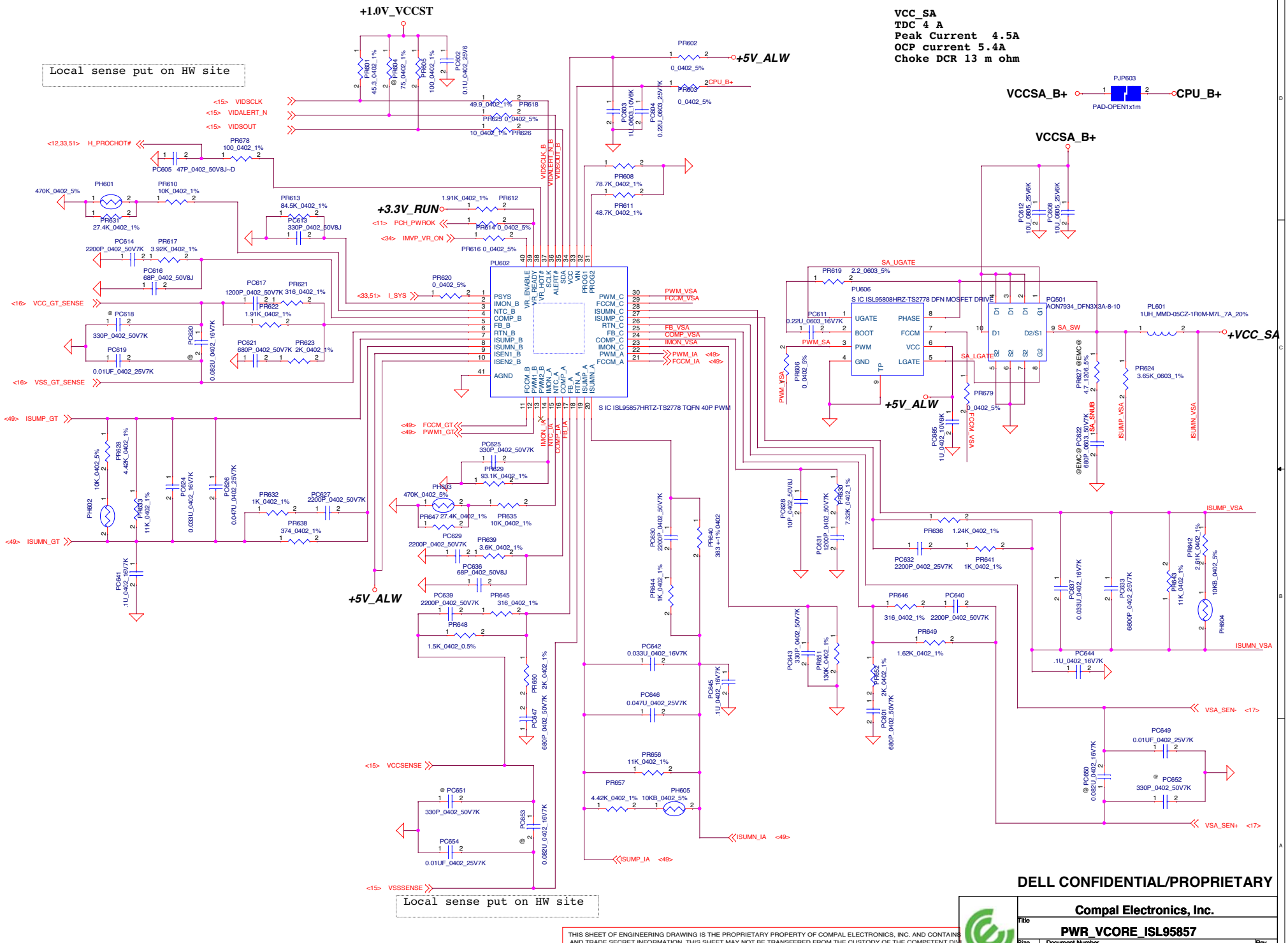
Date: Monday, April 25, 2016 | Sheet 47 of 52


+1.0V_VCCST
Local sense put on HW site
VCC_SA
TDC 4 A
Peak Current 4.5A
OCP current 5.4A
Choke DCR 13 m ohm
VCCSA_B+
CPU_B+
PJP603
PAD-OPEN1x1m
+5V_ALW
+3.3V_RUN
PU602
S IC ISL95857HRTZ-TS2778 TQFN 40P PWM
PU606
S IC ISL95808HRZ-TS2778 DFN MOSFET DRIVE
PQ501
AON7934_DFN3X3A-8-10
PL601
1UH_MMD-05CZ-1R0M-M7L_7A_20%
+VCC_SA
VSA_SEN-
VSA_SEN+
ISUMP_VSA
ISUMN_VSA
ISUMP_IA
ISUMN_IA
VCCSENSE
VSSSENSE
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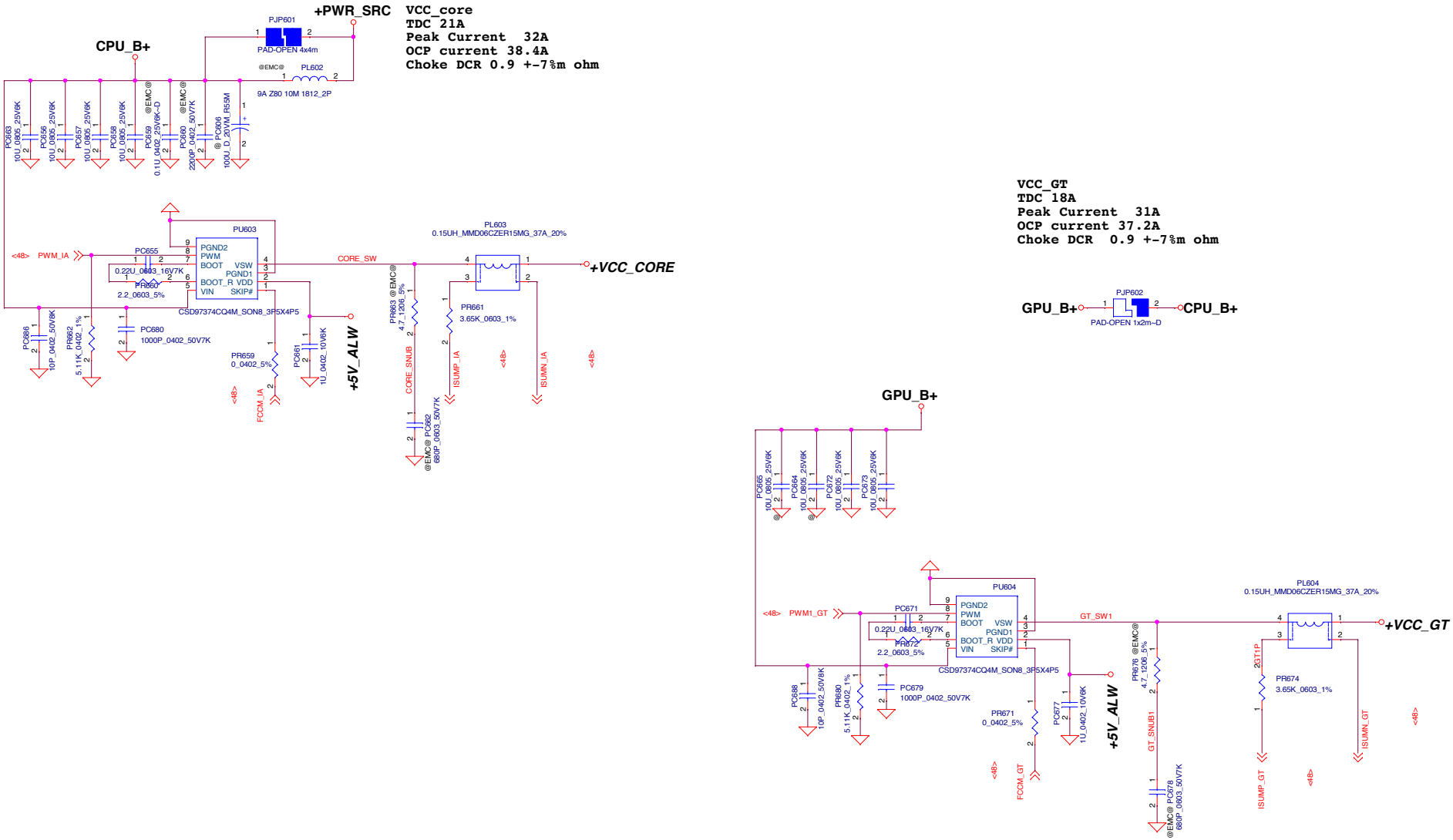
Compal Electronics, Inc.
PWR_VCORE_ISL95857
LA-Cxxxx
Monday, April 25, 2016



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Title: PWR_VCORE_ISL95857

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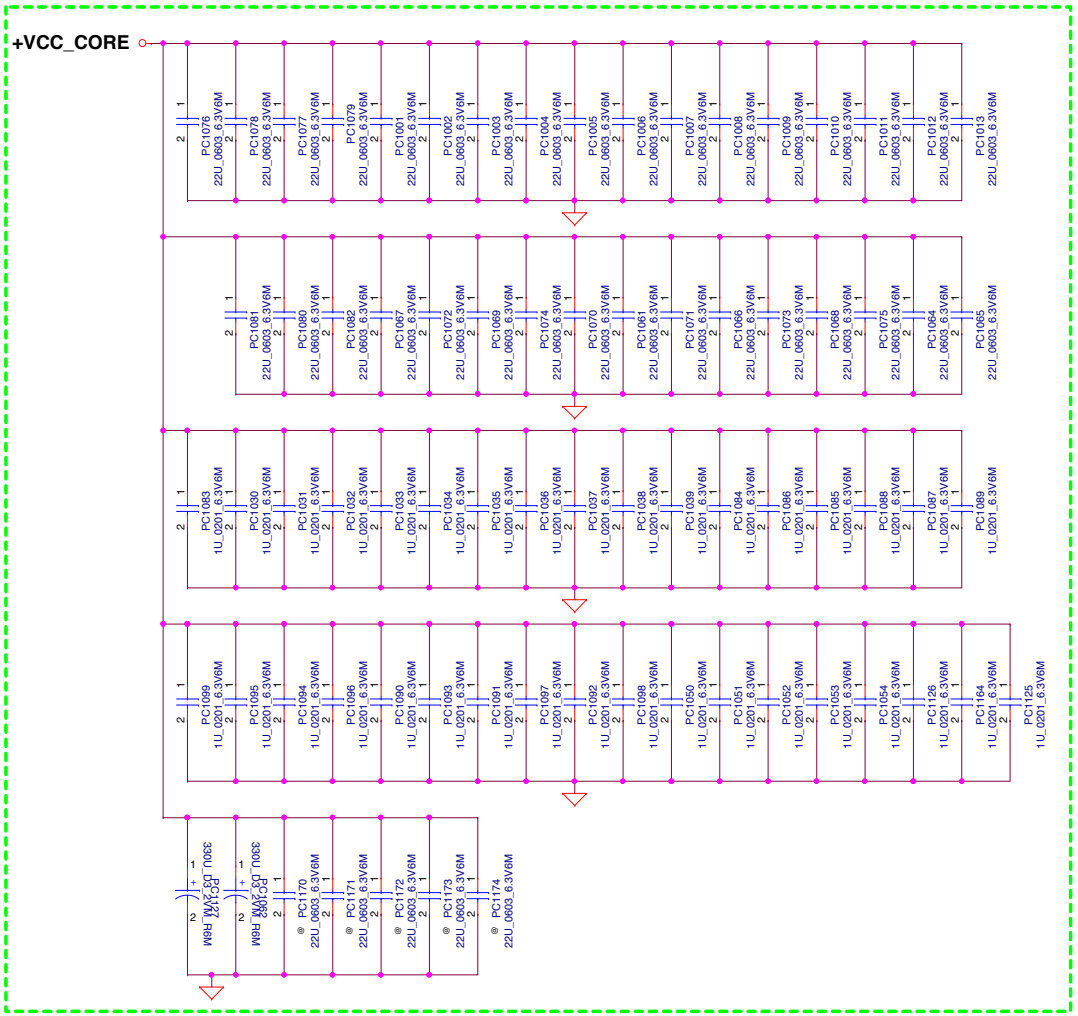
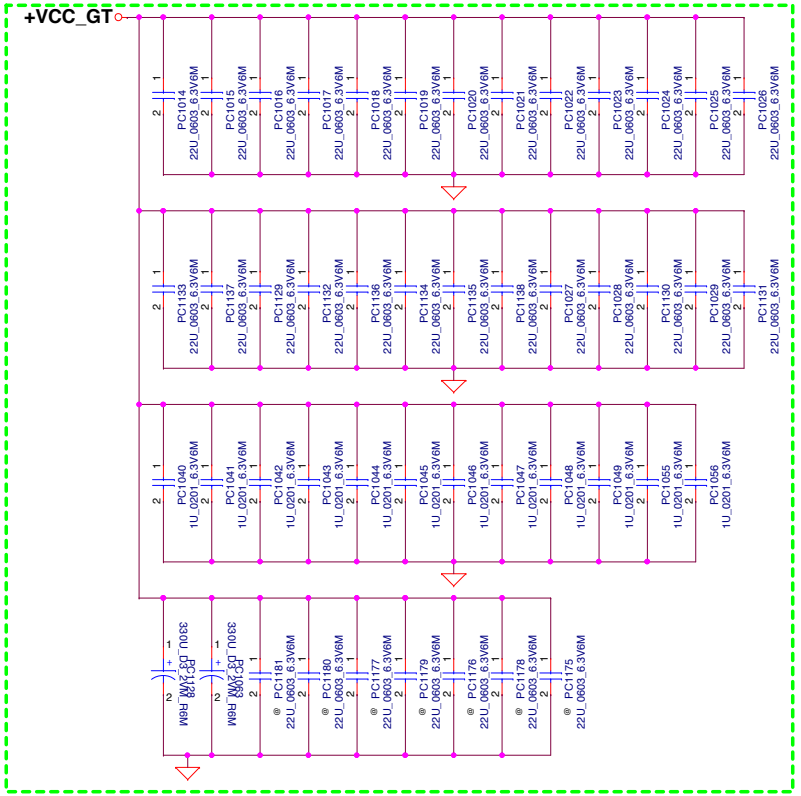
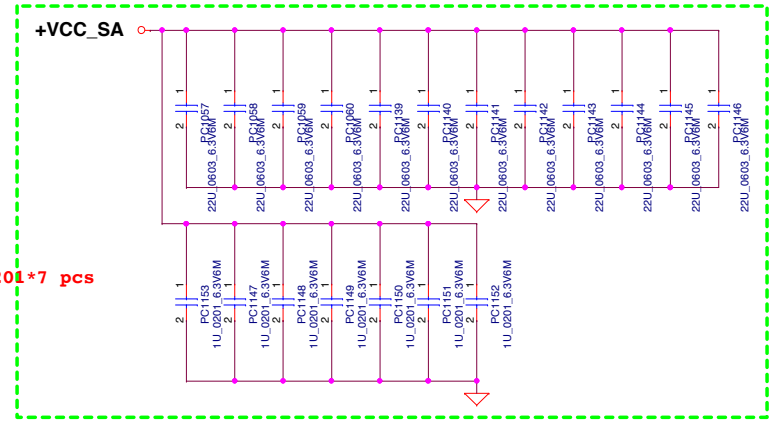
VCC_CORE Place on CPU
22U_0603 * 33 pcs +1U_0201*35 pcs
+330u_D2*2 pcs



VCC_GT Place on CPU (U22)
22U_0603 * 26 pcs +1U_0201*12 pcs
+330u_D2*2 pcs





VCC_SA Place on CPU
22U_0603 * 12 pcs + 1U_0201*7 pcs

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Title: PROCESSOR DECOUPLING

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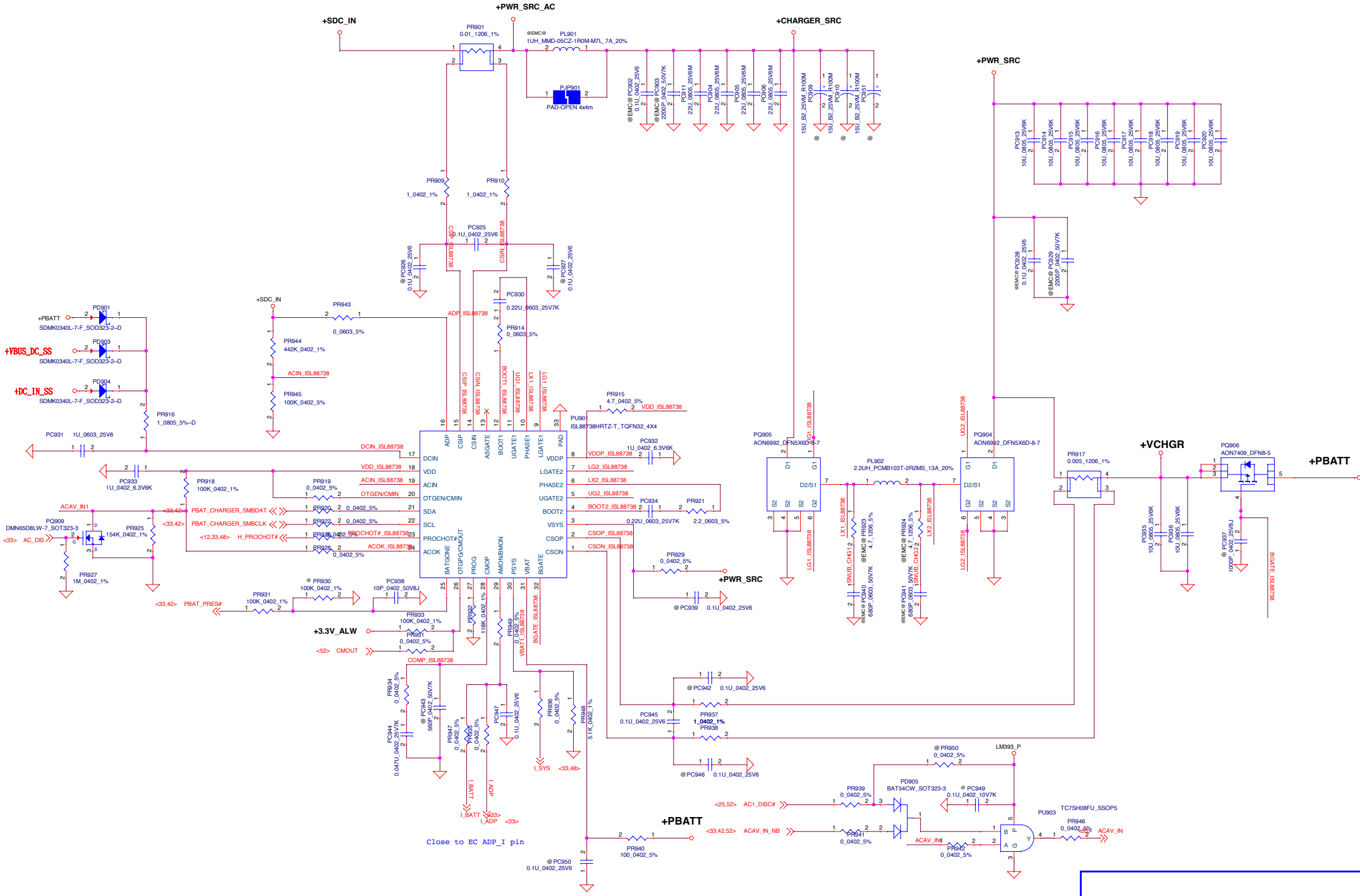
+SDC_IN
+PWR_SRC_AC
+CHARGER_SRC
+PWR_SRC
+PBATT
+VBUS_DC_SS
+DC_IN_SS
+VCHGR
+3.3V_ALW
PR901 0.01_1206_1%
@EMC@ PL901 1UH_MMD-05CZ-1R0M-M7L_7A_20%
PJP901 PAD-OPEN 4x4m
PR909 1_0402_1%
PR910 1_0402_1%
PC925 0.1U_0402_25V6
PD901 SDMK0340L-7-F_SOD323-2-D
PD903 SDMK0340L-7-F_SOD323-2-D
PD904 SDMK0340L-7-F_SOD323-2-D
PR916 1_0805_5%~D
PC931 1U_0603_25V6
PR943 0_0603_5%
PR944 442K_0402_1%
PR945 100K_0402_5%
PC930 0.22U_0603_25V7K
PR914 0_0603_5%
PU901 ISL88738HRTZ-T_TQFN32_4X4
PR915 4.7_0402_5%
PC932 1U_0402_6.3V6K
PC933 1U_0402_6.3V6K
PR918 100K_0402_1%
PR919 0_0402_5%
PR920 0_0402_5%
PR921 2.2_0603_5%
PC934 0.22U_0603_25V7K
PR922 0_0402_5%
PR923 0_0402_5%
PR924 0_0402_5%
PR925 154K_0402_1%
PR926 0_0402_5%
PC938 10P_0402_50V8J
PR927 1M_0402_1%
PR929 0_0402_5%
PR930 100K_0402_1%
PR931 100K_0402_1%
PR932 118K_0402_1%
PR933 100K_0402_1%
PR934 0_0402_5%
PC943 560P_0402_50V7K
PC944 0.047U_0402_25V7K
PR947 0_0402_5%
PR935 0_0402_5%
PC947 0.1U_0402_25V6
PR936 0_0402_5%
PR948 5.1K_0402_1%
PR940 100_0402_5%
PC950 0.1U_0402_25V6
PC945 0.1U_0402_25V6
PR937 1_0402_1%
PR938
PC942 0.1U_0402_25V6
PC946 0.1U_0402_25V6
PC939 0.1U_0402_25V6
PQ905 AON6992_DFN5X6D-8-7
PQ904 AON6992_DFN5X6D-8-7
PL902 2.2UH_PCMB103T-2R2MS_13A_20%
PR917 0.005_1206_1%
PQ906 AON7409_DFN8-5
PC935 10U_0805_25V6K
PC936 10U_0805_25V6K
PC937 1000P_0402_25V8J
PR950 0_0402_5%
PD905 BAT54CW_SOT323-3
PR939 0_0402_5%
PR941 0_0402_5%
PR942 0_0402_5%
PC949 0.1U_0402_10V7K
PU903 TC7SH08FU_SSOP5
PR946 0_0402_5%
PC913 10U_0805_25V6K
PC914 10U_0805_25V6K
PC915 10U_0805_25V6K
PC916 10U_0805_25V6K
PC917 10U_0805_25V6K
PC918 10U_0805_25V6K
PC919 10U_0805_25V6K
PC920 10U_0805_25V6K
@EMC@ PC928 0.1U_0402_25V6
@EMC@ PC929 2200P_0402_50V7K
@EMC@ PC902 0.1U_0402_25V6
@EMC@ PC903 2200P_0402_50V7K
PC911 22U_0805_25V6M
PC904 22U_0805_25V6M
PC905 22U_0805_25V6M
PC906 22U_0805_25V6M
PC907 22U_0805_25V6M
15U_B2_25VM_R100M
@EMC@ PC940 680P_0603_50V7K
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@EMC@ PR924 4.7_1206_5%
PC926 0.1U_0402_25V6
PC927 0.1U_0402_25V6
PC908 0.1U_0402_25V6
PR909 1_0402_1%
PR910 1_0402_1%
PR914 0_0603_5%
PR915 4.7_0402_5%
PR916 1_0805_5%~D
PR917 0.005_1206_1%
PR918 100K_0402_1%
PR919 0_0402_5%
PR920 0_0402_5%
PR921 2.2_0603_5%
PR922 0_0402_5%
PR923 0_0402_5%
PR924 0_0402_5%
PR925 154K_0402_1%
PR926 0_0402_5%
PR927 1M_0402_1%
PR929 0_0402_5%
PR930 100K_0402_1%
PR931 100K_0402_1%
PR932 118K_0402_1%
PR933 100K_0402_1%
PR934 0_0402_5%
PR935 0_0402_5%
PR936 0_0402_5%
PR937 1_0402_1%
PR938
PR939 0_0402_5%
PR940 100_0402_5%
PR941 0_0402_5%
PR942 0_0402_5%
PR946 0_0402_5%
PR947 0_0402_5%
PR948 5.1K_0402_1%
PR949 0_0402_5%
PR950 0_0402_5%
PC901 1U_0402_6.3V6K
PC902 0.1U_0402_25V6
PC903 2200P_0402_50V7K
PC904 22U_0805_25V6M
PC905 22U_0805_25V6M
PC906 22U_0805_25V6M
PC907 22U_0805_25V6M
PC908 0.1U_0402_25V6
PC909 0.1U_0402_25V6
PC910 22U_0805_25V6M
PC911 22U_0805_25V6M
PC912 0.1U_0402_25V6
PC913 10U_0805_25V6K
PC914 10U_0805_25V6K
PC915 10U_0805_25V6K
PC916 10U_0805_25V6K
PC917 10U_0805_25V6K
PC918 10U_0805_25V6K
PC919 10U_0805_25V6K
PC920 10U_0805_25V6K
PC921 2.2_0603_5%
PC922 0.1U_0402_25V6
PC923 0.1U_0402_25V6
PC924 0.1U_0402_25V6
PC925 0.1U_0402_25V6
PC926 0.1U_0402_25V6
PC927 0.1U_0402_25V6
PC928 0.1U_0402_25V6
PC929 2200P_0402_50V7K
PC930 0.22U_0603_25V7K
PC931 1U_0603_25V6
PC932 1U_0402_6.3V6K
PC933 1U_0402_6.3V6K
PC934 0.22U_0603_25V7K
PC935 10U_0805_25V6K
PC936 10U_0805_25V6K
PC937 1000P_0402_25V8J
PC938 10P_0402_50V8J
PC939 0.1U_0402_25V6
PC940 680P_0603_50V7K
PC941 680P_0603_50V7K
PC942 0.1U_0402_25V6
PC943 560P_0402_50V7K
PC944 0.047U_0402_25V7K
PC945 0.1U_0402_25V6
PC946 0.1U_0402_25V6
PC947 0.1U_0402_25V6
PC948 0.1U_0402_25V6
PC949 0.1U_0402_10V7K
PC950 0.1U_0402_25V6
PD901 SDMK0340L-7-F_SOD323-2-D
PD903 SDMK0340L-7-F_SOD323-2-D
PD904 SDMK0340L-7-F_SOD323-2-D
PD905 BAT54CW_SOT323-3
PJP901 PAD-OPEN 4x4m
PL901 1UH_MMD-05CZ-1R0M-M7L_7A_20%
PL902 2.2UH_PCMB103T-2R2MS_13A_20%
PQ901 DMN65D8LW-7_SOT323-3
PQ904 AON6992_DFN5X6D-8-7
PQ905 AON6992_DFN5X6D-8-7
PQ906 AON7409_DFN8-5
PU901 ISL88738HRTZ-T_TQFN32_4X4
PU903 TC7SH08FU_SSOP5
DCIN
VDD
ACIN
OTGEN/CMIN
SDA
SCL
PROCHOT#
ACOK
ADP
CSIP
CSIN
ASGATE
BOOT1
UGATE1
PHASE1
LGATE1
PAD
VDDP
LGATE2
PHASE2
UGATE2
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VSYS
CSOP
CSON
BATGONE
OTGPG/CMOUT
PROG
CMOP
AMON/BMON
PSYS
VBAT
BGATE
ACAV_IN1
AC_DIS
PBAT_PRES#
PBAT_CHARGER_SMBDAT
PBAT_CHARGER_SMBCLK
H_PROCHOT#
ACOK_ISL88738
CMOUT
COMP_ISL88738
I_SYS
I_BATT
I_ADP
Close to EC ADP_I pin
AC1_DISC#
ACAV_IN_NB
ACAV_IN
LM393_P
Security Classification
Compal Secret Data
Issued Date
2014/10/24
Deciphered Date
2015/08/31
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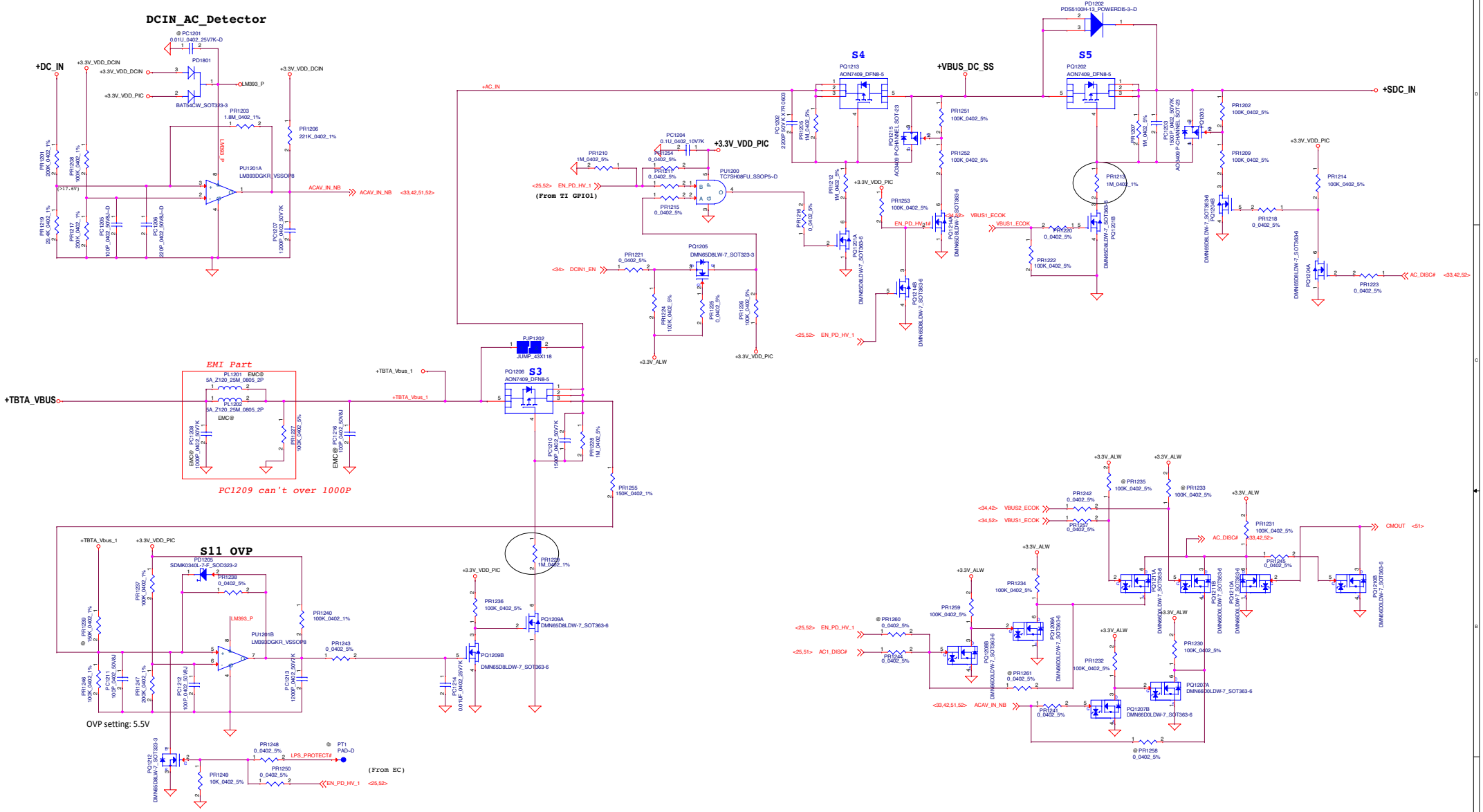
Compal Electronics, Inc.
Title
P47-PWR_CHARGER ISL9237 (Colay)
Size
Document Number
LA-D161P
Rev
0.1
Date: Monday, April 25, 2016
Sheet 51 of 52



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